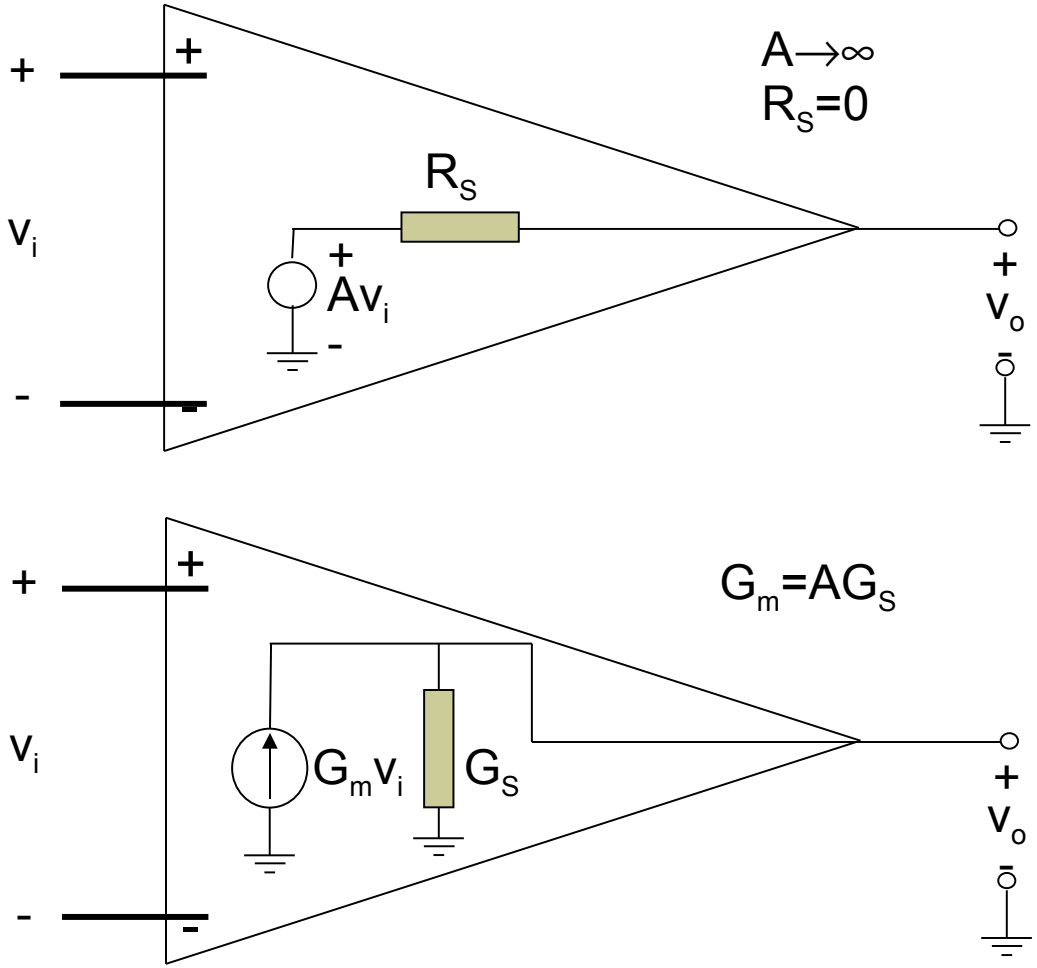
CAPÍTULO 5

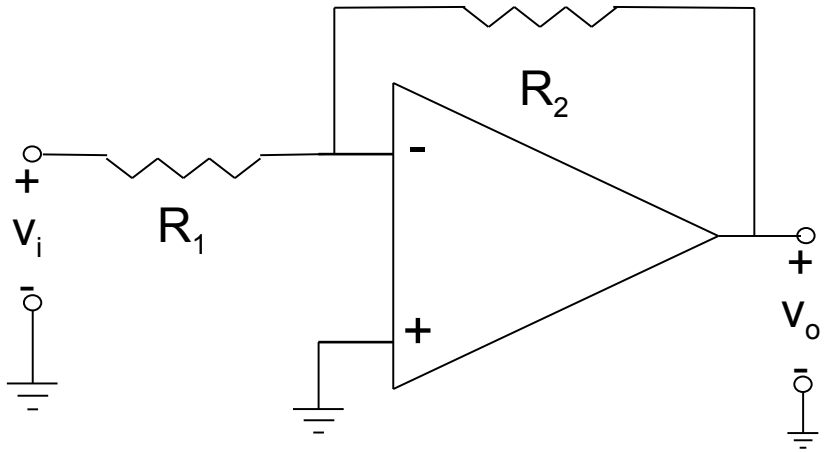
AMPLIFICADORES OPERACIONAIS CMOS

5.1 Introdução

amp op ideal

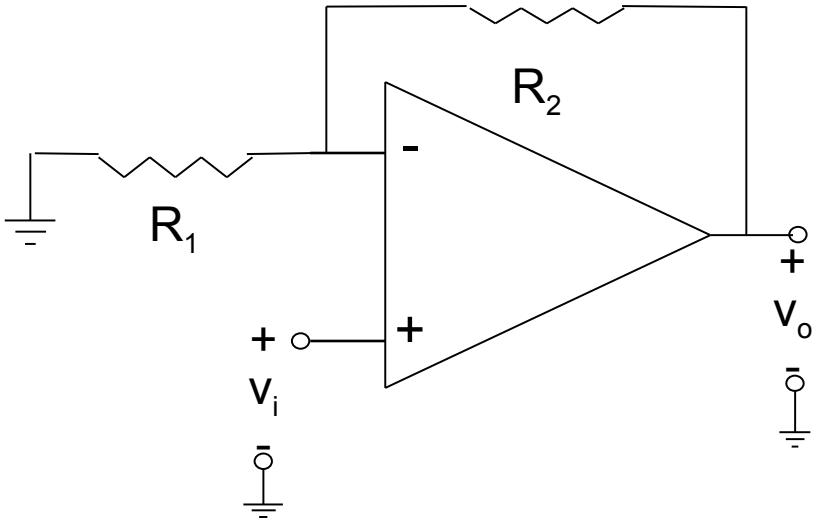


Aplicações



amplificador inversor

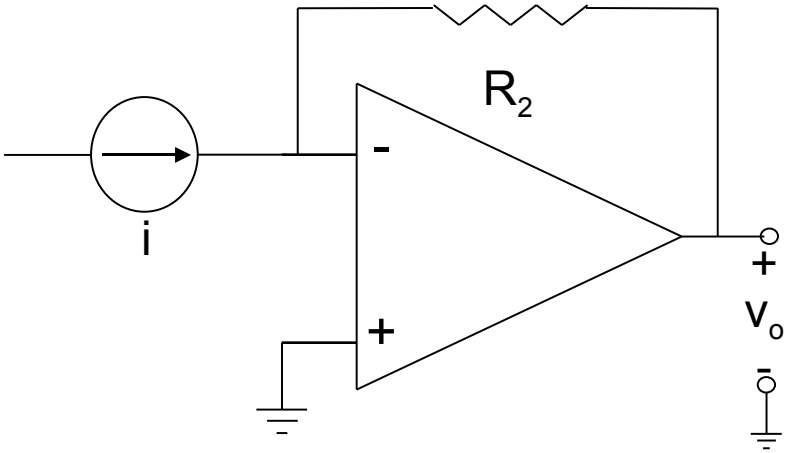
$$\frac{v_o}{v_i} = -\frac{R_2}{R_1}\frac{1}{1+\frac{1}{A}\left(1+\frac{R_2}{R_1}\right)} \cong -\frac{R_2}{R_1}$$



amplificador não inversor

$$\frac{v_o}{v_i} = \left(1+\frac{R_2}{R_1}\right)\frac{1}{1+\frac{1}{A}\left(1+\frac{R_2}{R_1}\right)} \cong 1+\frac{R_2}{R_1}$$

Aplicações - 2



Transimpedance amplifier

$$\frac{v_o}{i} = -R_2 \frac{A}{1+A} \cong -R_2\left(1-\frac{1}{A}\right) \cong -R_2$$

- Continuous-time filters
- SC filters
- D/A & A/D converters
- Sensor signal conditioning
- Voltage & current references
- Comparators
- Nonlinear analog functions,
- .....

Requisitos de projeto:

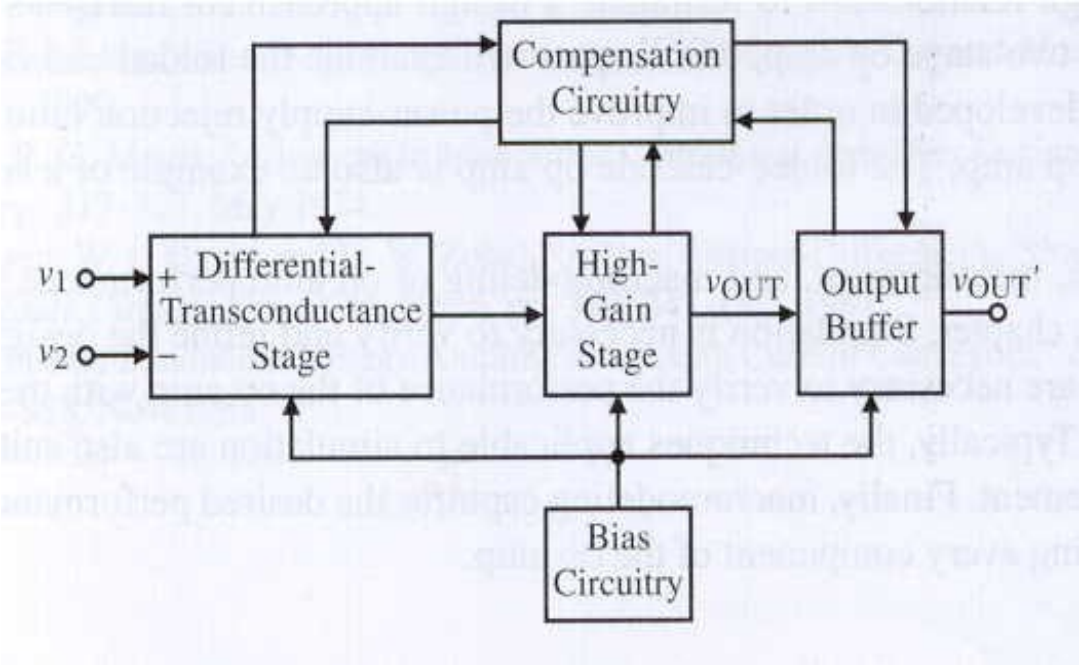
Tecnologia;

- **Tensão de Alimentação;**
- **Ganho, GBW, excursão de tensão na saída, ruído, tensão de offset, CMRR, PSRR, ICMR, SR ...**

Etapas de projeto:

- **Escolha da arquitetura;**
- **Correntes de polarização & dimensões dos transistores;**
- **Compensação;**
- **Simulação;**
- **Layout;**
- **Simulação pós-layout**

Diagrama em blocos de um amp. op. genérico



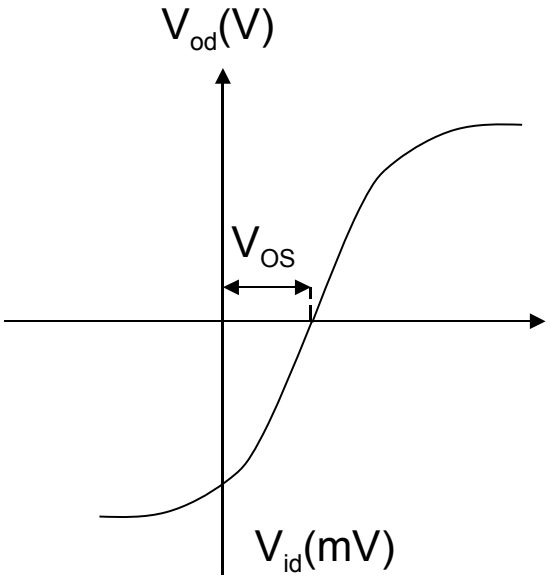
P. Allen and D. Holberg – CMOS Analog Circuit Design, 2nd. Ed., Oxford, New York, 2002.

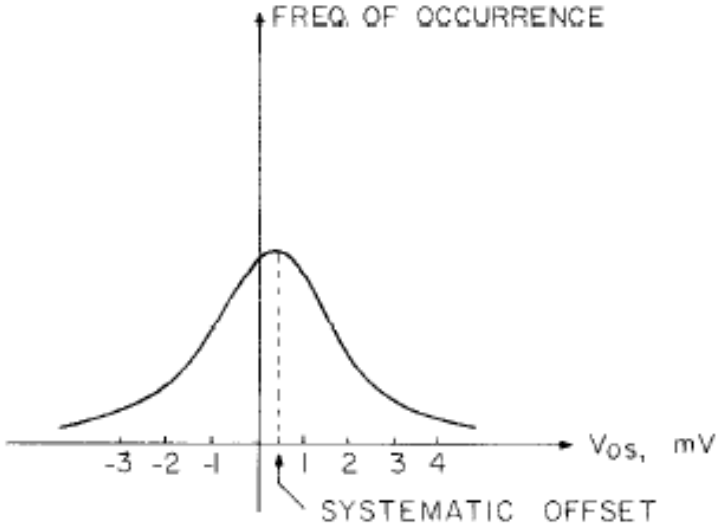
5.2 Parametros de Desempenho

TABLE 6.1-2 Specifications for a Typical Unbuffered CMOS Op Amp

Boundary Conditions	Requirement
Process specification	See Tables 3.1-1, 3.1-2, and 3.2-1
Supply voltage	± 2.5 V $\pm 10\%$
Supply current	100 μA
Temperature range	0–70 °C
Specifications	
Gain	$\geq$ 70 dB
Gain bandwidth	$\geq$ 5 MHz
Settling time	$\leq$ 1 μs
Slew rate	$\geq$ 5 V/μs
ICMR	$\geq \pm 1.5$ V
CMRR	$\geq$ 60 dB
PSRR	$\geq$ 60 dB
Output swing	$\geq \pm 1.5$ V
Output resistance	N/A, capacitive load only
Offset	$\leq \pm 10$ mV
Noise	$\leq 100\ \text{nV}/\sqrt{\text{Hz}}$ at 1 kHz
Layout area	$\leq 5000 \times (\text{minimum channel length})^2$

Tensão de Offset



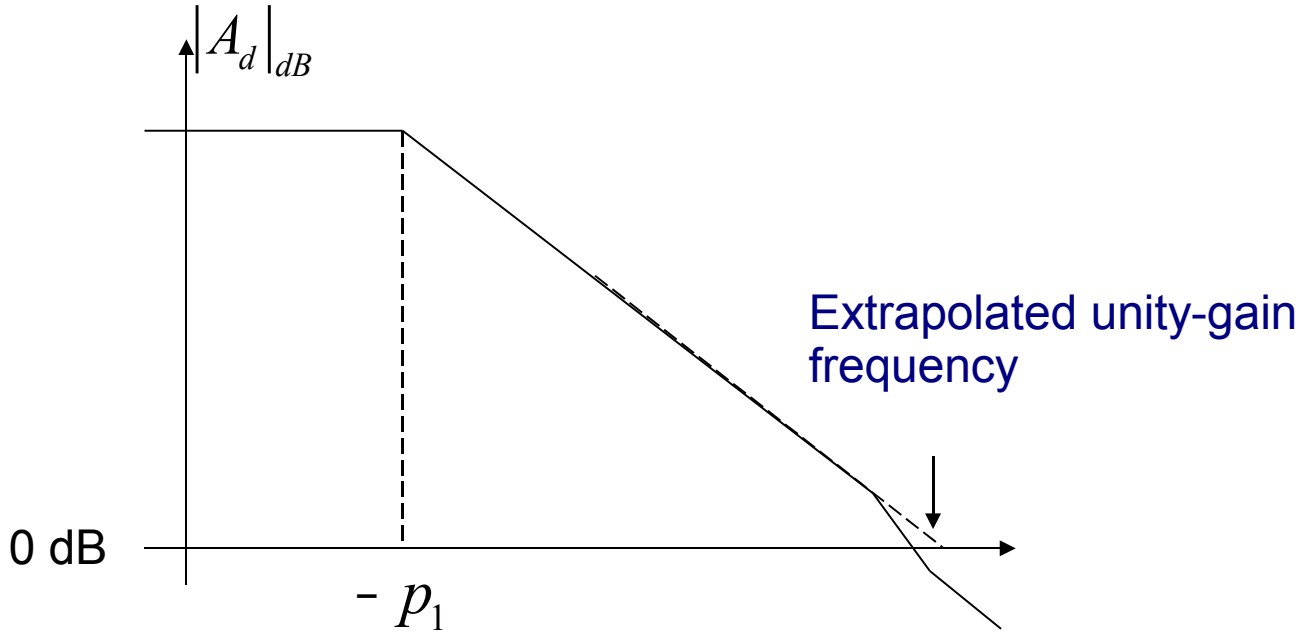


Typical input offset distribution, MOS operational amplifier.

Offset sistemático – é resultado do projeto do circuito e está presente mesmo quando todos os dispositivos supostamente idênticos são casados (geralmente pode-se obter baixos valores).

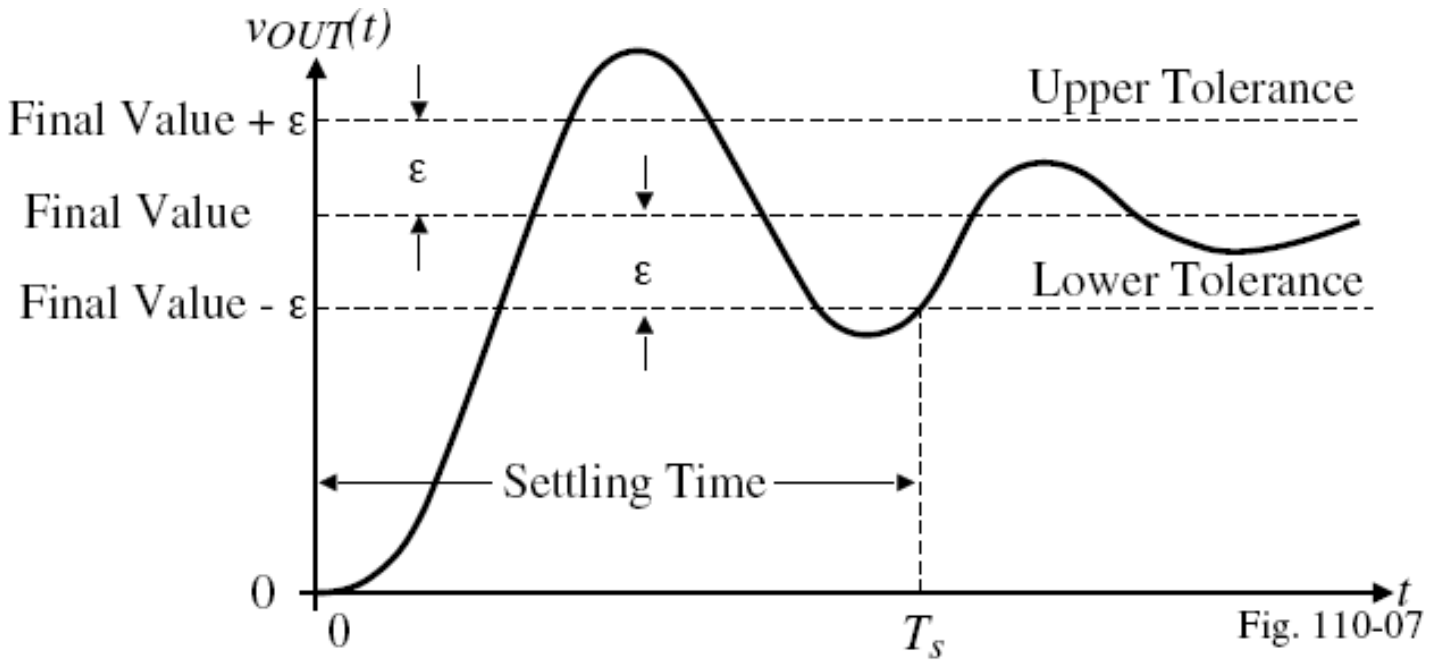
Offset randômico – é resultado dos descasamentos nos pares de dispositivos supostamente idênticos (depende da área e da polarização).

Ganho de Tensão Diferencial



P. R. Gray and R. G. Meyer, MOS Operational Amplifier Design – A Tutorial Overview, IEEE JSSC, vo. 17, n0. 6, pp. 969-982, Dec. 1982.

Tempo de Acomodação (*Settling time*)



P. Allen and D. Holberg – CMOS Analog Circuit Design, 2nd. Ed., Oxford, New York, 2002.

Outros Parâmetros de Desempenho

CMRR, PSRR, Slew rate, Noise, Common-Mode Input Range, Output Swing, Power, Silicon Real State, ...

Faixa Dinâmica (Dynamic Range) - DR

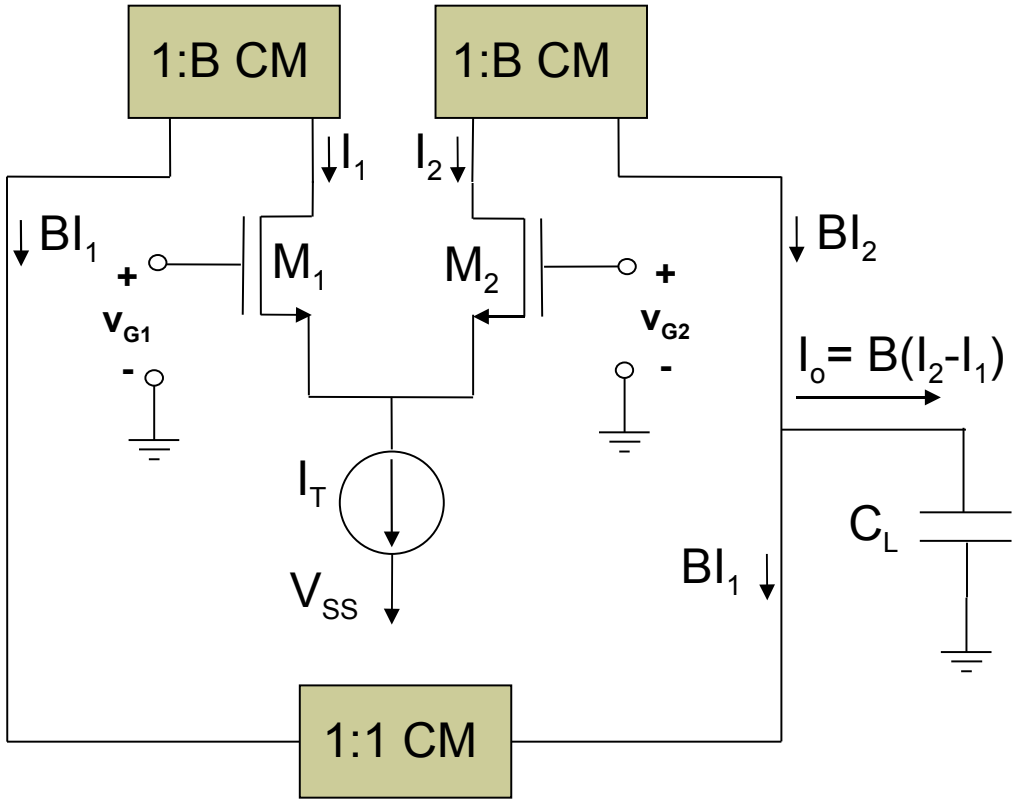
Distorção (dentro de um nível aceitável: depende da aplicação).

$$DR = 20\log\left(\frac{v_{in,\max}}{v_{in,\min}}\right)$$

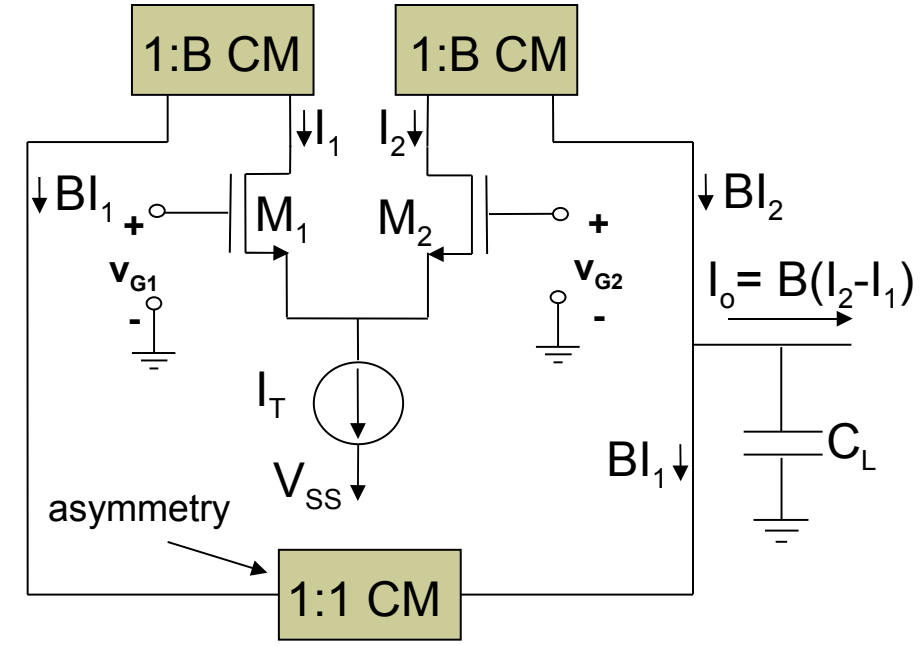
Ruído (distinção entre sinal e ruído)

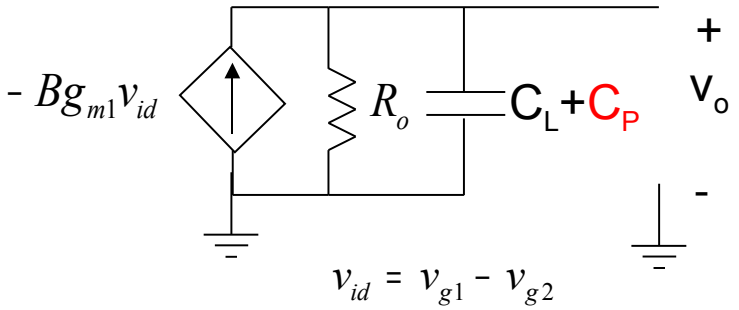
5.3 OTA (amp op de um estágio)

OTA – Amplificador Operacional de Transcondutância



Faixa de modo comum na entrada = amp. dif.

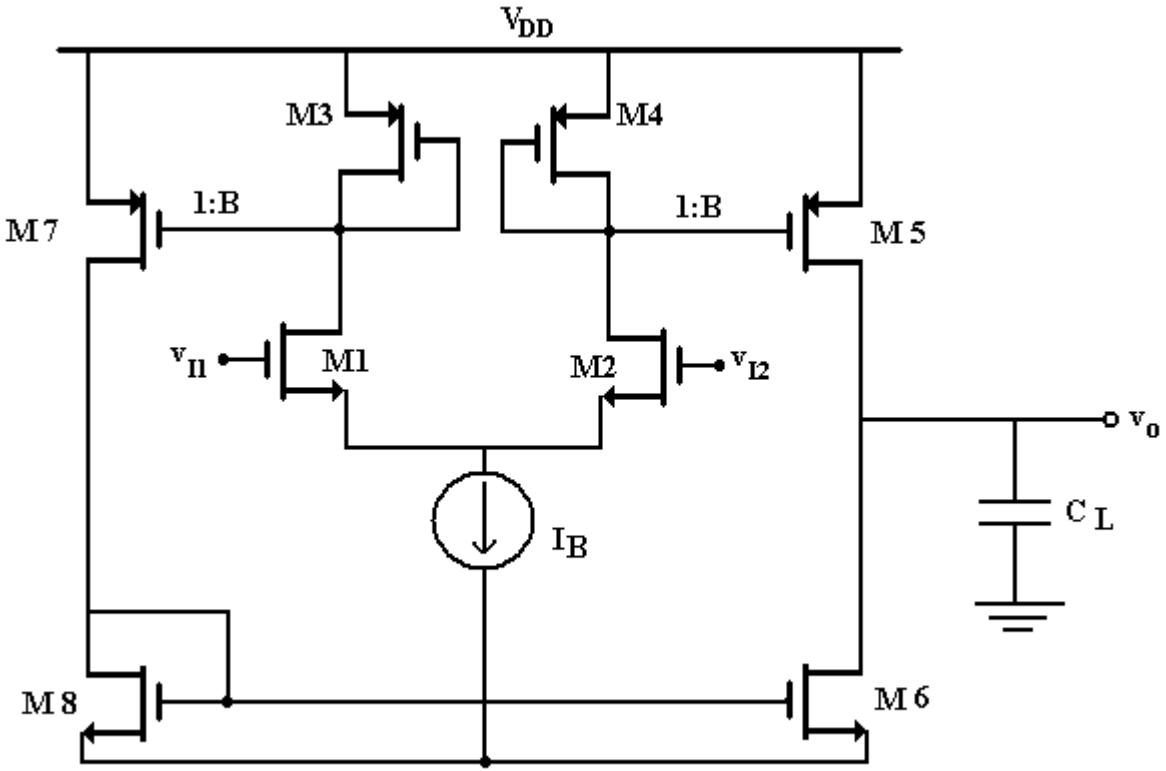




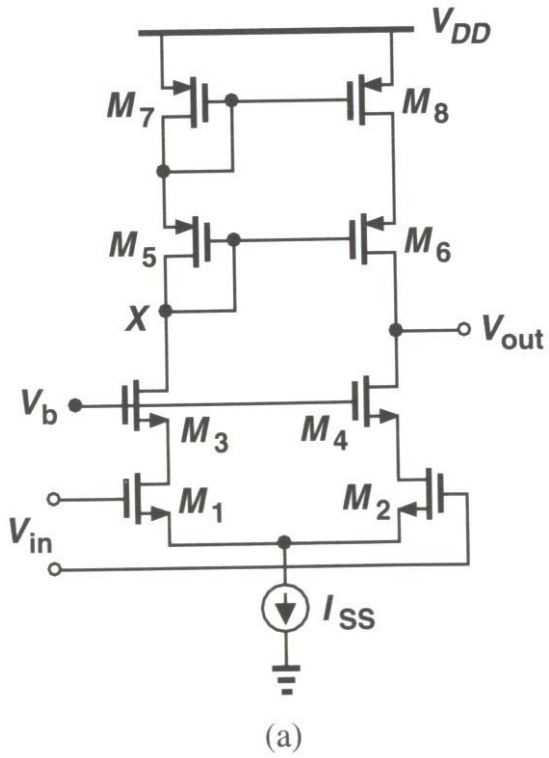
$$SR = \frac{BI_T}{(C_L + C_P)}$$

$$A_d(s) = \frac{Bg_{m1}R_o}{1 + sR_o(C_L + C_P)}$$

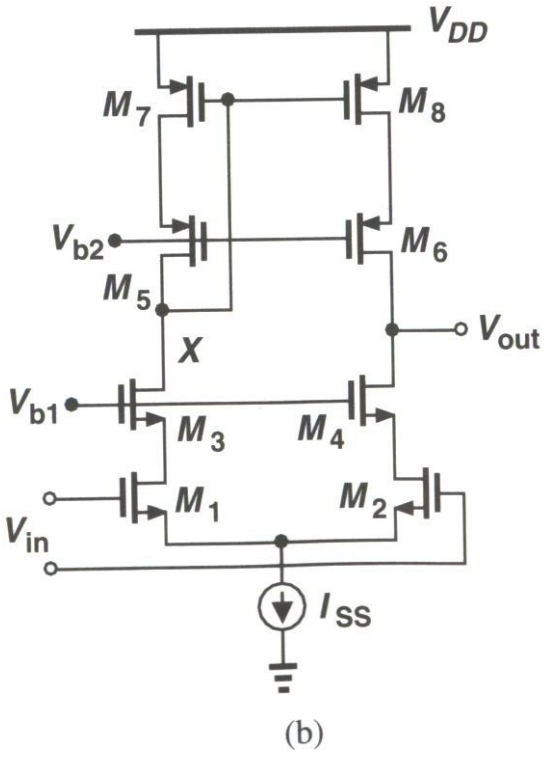
$$GBW(Hz) = \frac{1}{2\pi}\frac{Bg_{m1}}{(C_L + C_P)}$$


V_{DD}
M3
M4
1:B
1:B
M7
M5
v_{I1}
M1
M2
v_{I2}
v_o
I_B
C_L
M8
M6

5.4 Amplificadores Cascode & Folded-Cascode



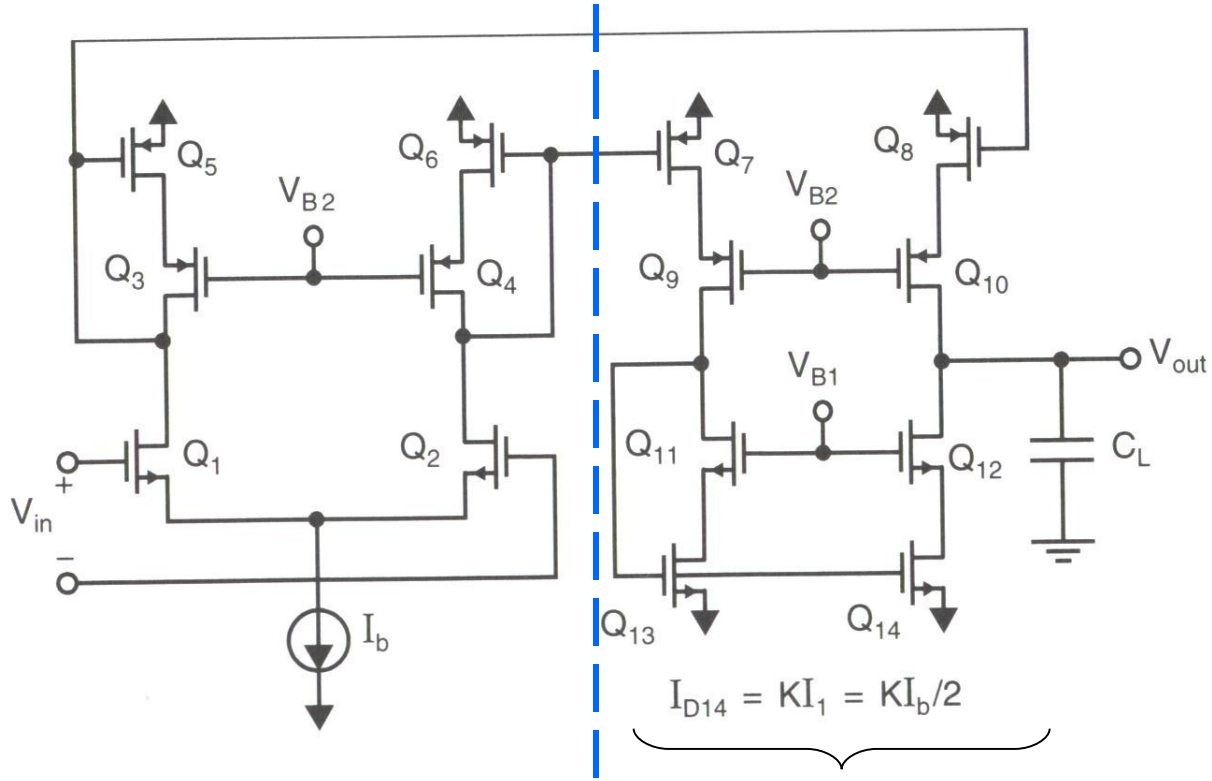
Amp. Dif. Telescópico amp. Com espelho cascode auto-polarizado



Amp. diff. Telescópico com espelho cascode de baixa tensão

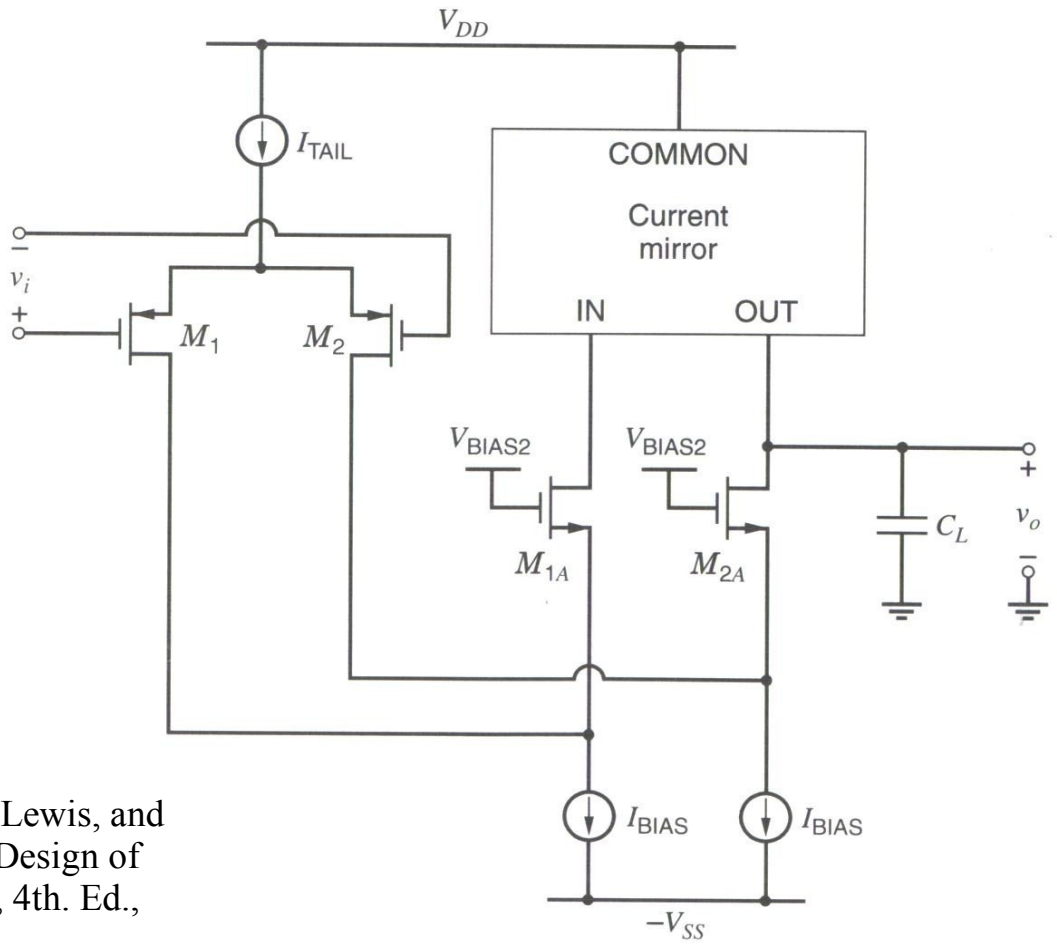
- Reduzida excursão de tensão;
- Doublet !
- Não adequado para para aplicações de baixa tensão

Amplificador folded-cascode



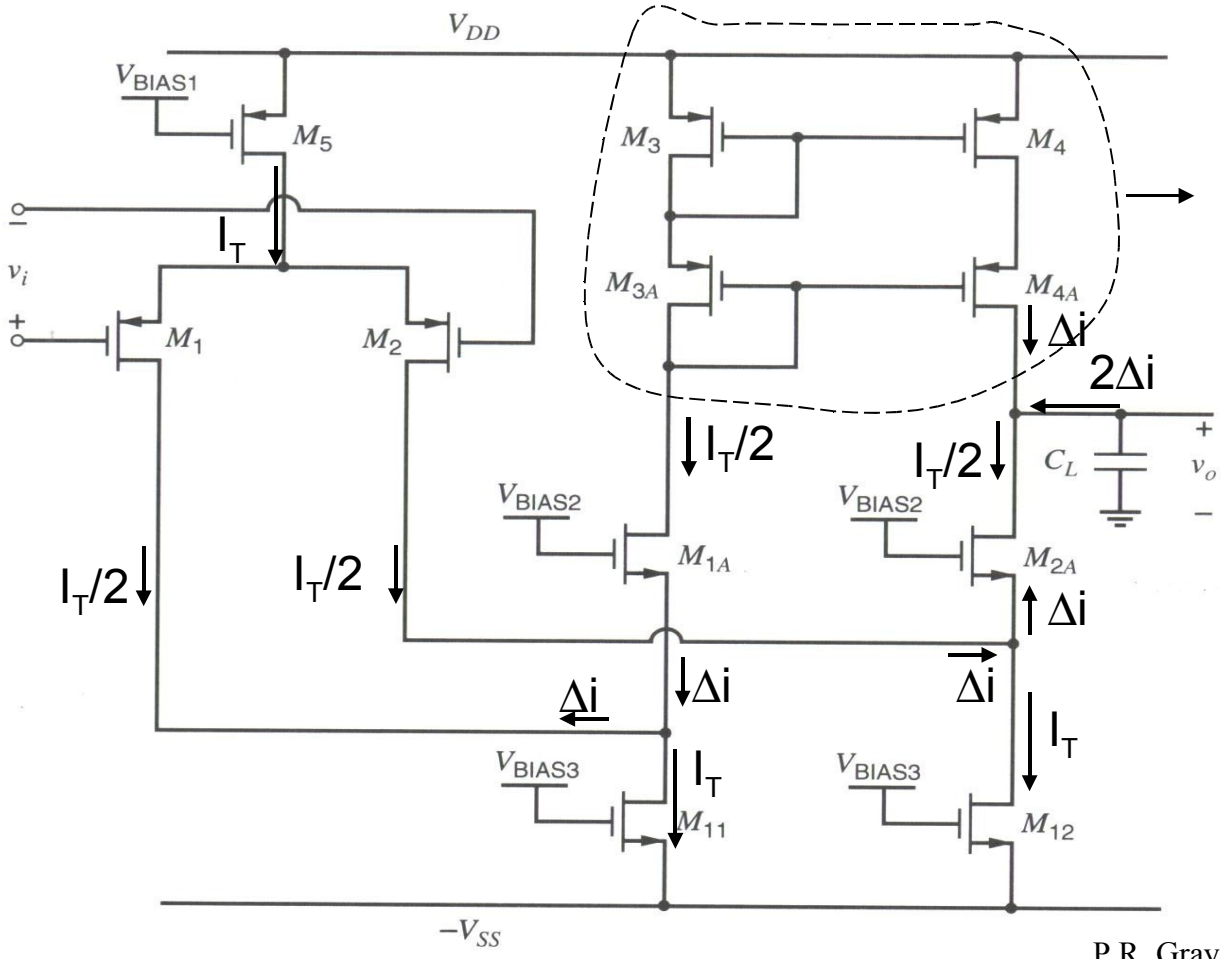
D. Johns and K. Martin, *Analog Integrated Circuit Design,* Wiley, 1997.

Amplificador folded-cascode



P.R. Gray, P.J. Hurst, S.H. Lewis, and R.G. Meyer, Analysis and Design of Analog Integrated Circuits, 4th. Ed., Wiley, 2001.

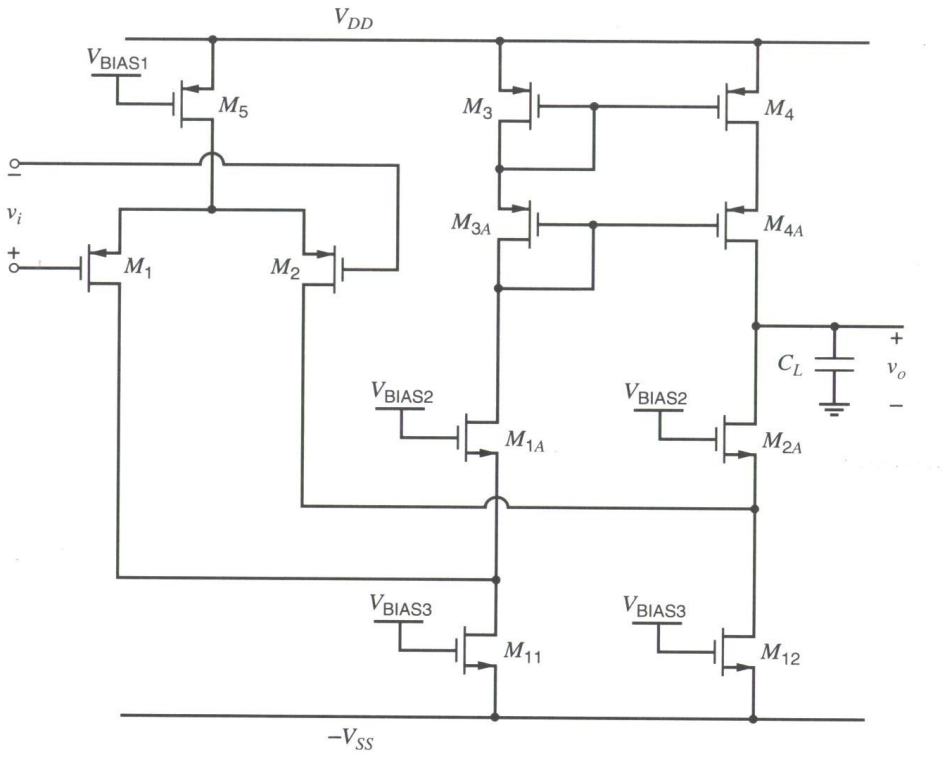
Amplificador folded-cascode



Pode ser alterado para aumentar a excursão de tensão

P.R. Gray, P.J. Hurst, S.H. Lewis, and R.G. Meyer, Analysis and Design of Analog Integrated Circuits, 4th. Ed., Wiley, 2001.

Amplificador folded-cascode



High-swing current mirror

$$SR^{\pm} = \pm \frac{I_T}{C_L}$$

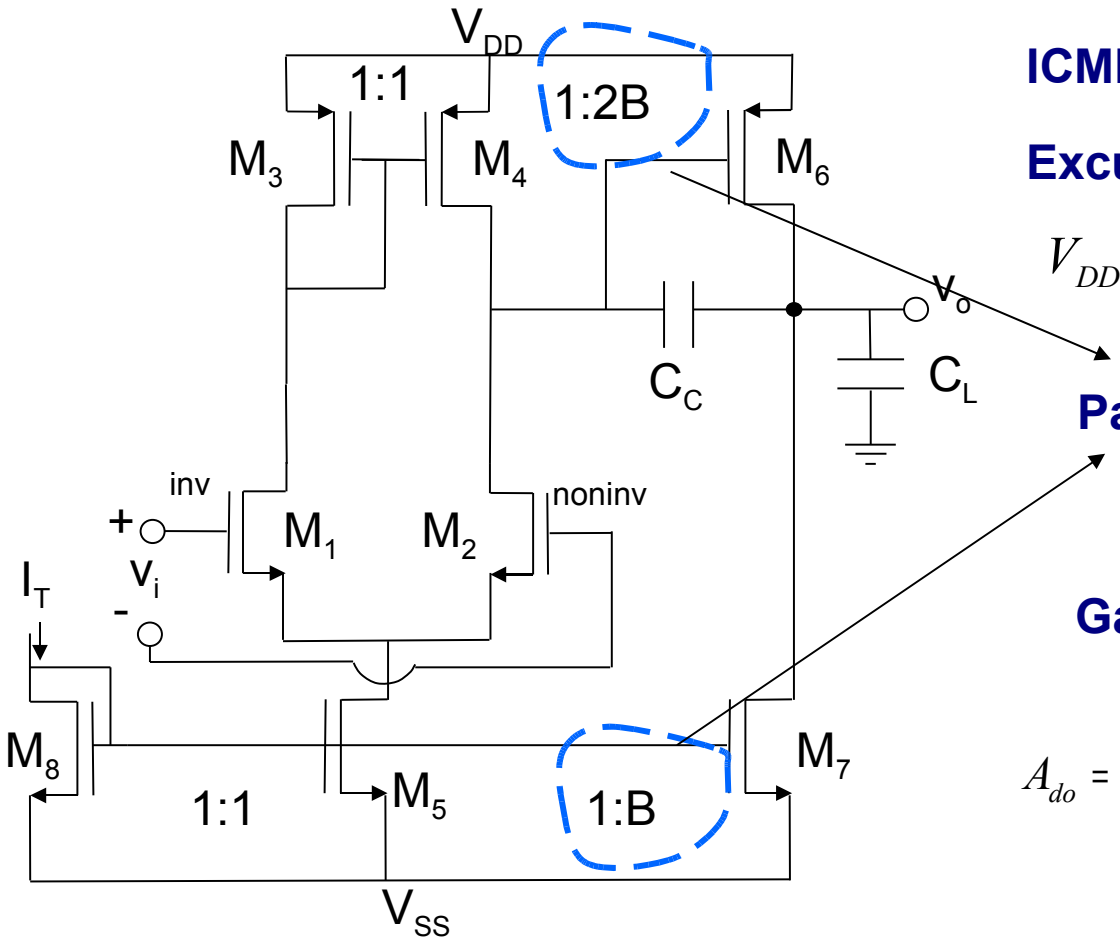
$$A_d \cong \frac{A_{d0}}{1 + sC_L R_0}$$ & doublet

$$A_{d0} = G_m R_o \qquad G_m = g_{m1}$$

$$G_o = \frac{1}{R_o} = g_{ds4} \frac{g_{ds4A}}{g_{ms4A}} + \left(g_{ds12} + g_{ds2} \right) \frac{g_{ds2A}}{g_{ms2A}}$$

P.R. Gray, P.J. Hurst, S.H. Lewis, and R.G. Meyer, Analysis and Design of Analog Integrated Circuits, 4th. Ed., Wiley, 2001.

5.5 Amplificador Operacional de dois estágios



ICMR: ver amp. dif.

Excursão de tensão na saída

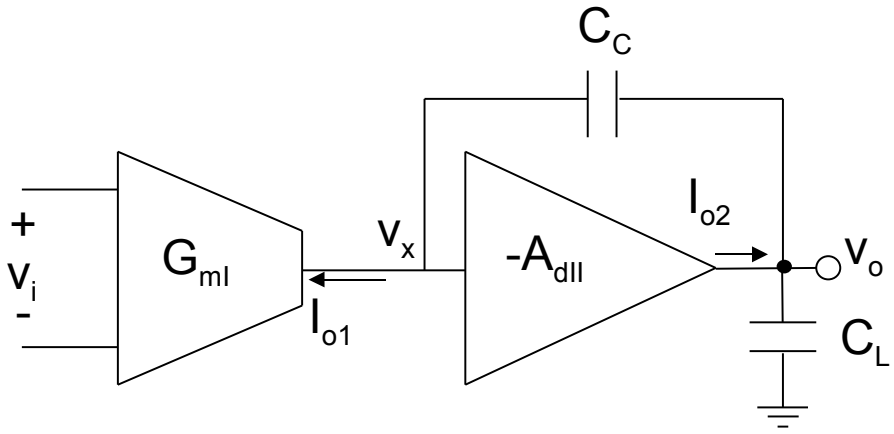
$$V_{DD} - V_{DSsat4} > V_o > V_{SS} + V_{DSsat5}$$

Para *offset* sistemático $\rightarrow$ 0.

Ganho de tensão:

$$A_{do} = \left.\frac{v_o}{v_i}\right|_{LF} = -\frac{g_{m1}}{g_{ds2} + g_{ds2}} \frac{g_{m6}}{g_{ds6} + g_{ds7}}$$

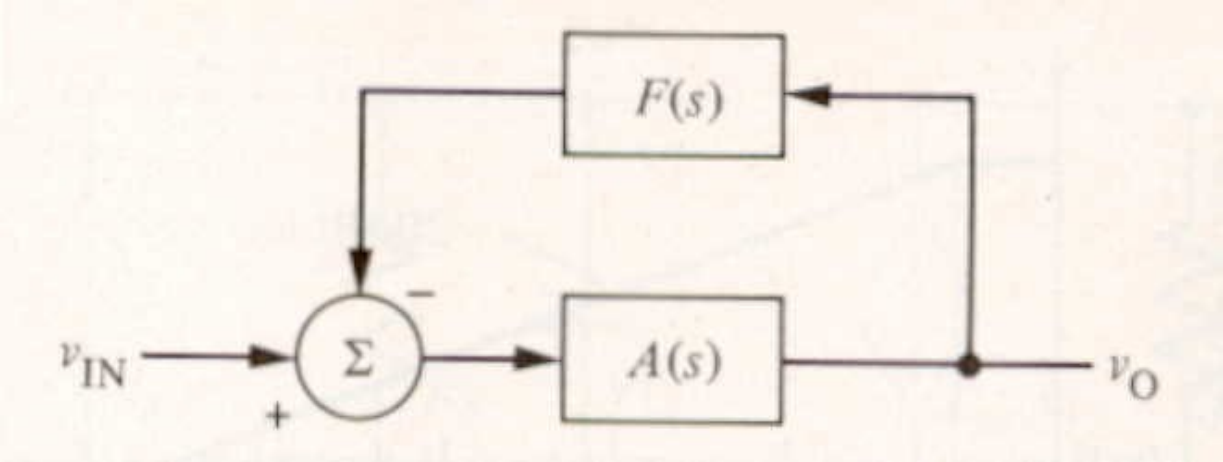
Amplificador Operacional de dois estágios



$$I_{o1} = C_C \frac{d\left(v_o - v_x\right)}{dt} \cong C_C \frac{dv_o}{dt} \rightarrow \frac{dv_o}{dt} = \frac{I_T}{C_C} \Rightarrow SR^{\pm} = \pm \frac{I_T}{C_C}$$

$$I_{o2} = I_{o1} + C_L \frac{dv_o}{dt} \rightarrow \frac{dv_o}{dt} = \frac{I_{o2} - I_{o1}}{C_L} \Rightarrow \begin{cases} SR^{+}_{ext} \cong \dfrac{I_{6\max} - (B+1)I_B}{C_L} > SR^{+} \\ SR^{-}_{ext} = -\dfrac{(B-1)I_T}{C_L} \end{cases}$$

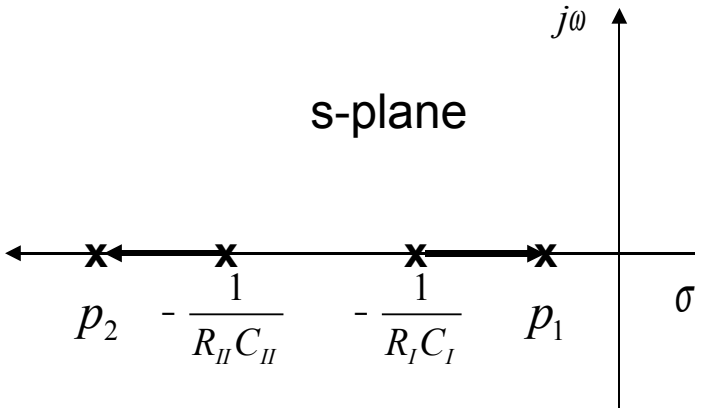
Amplificador Operacional de dois estágios



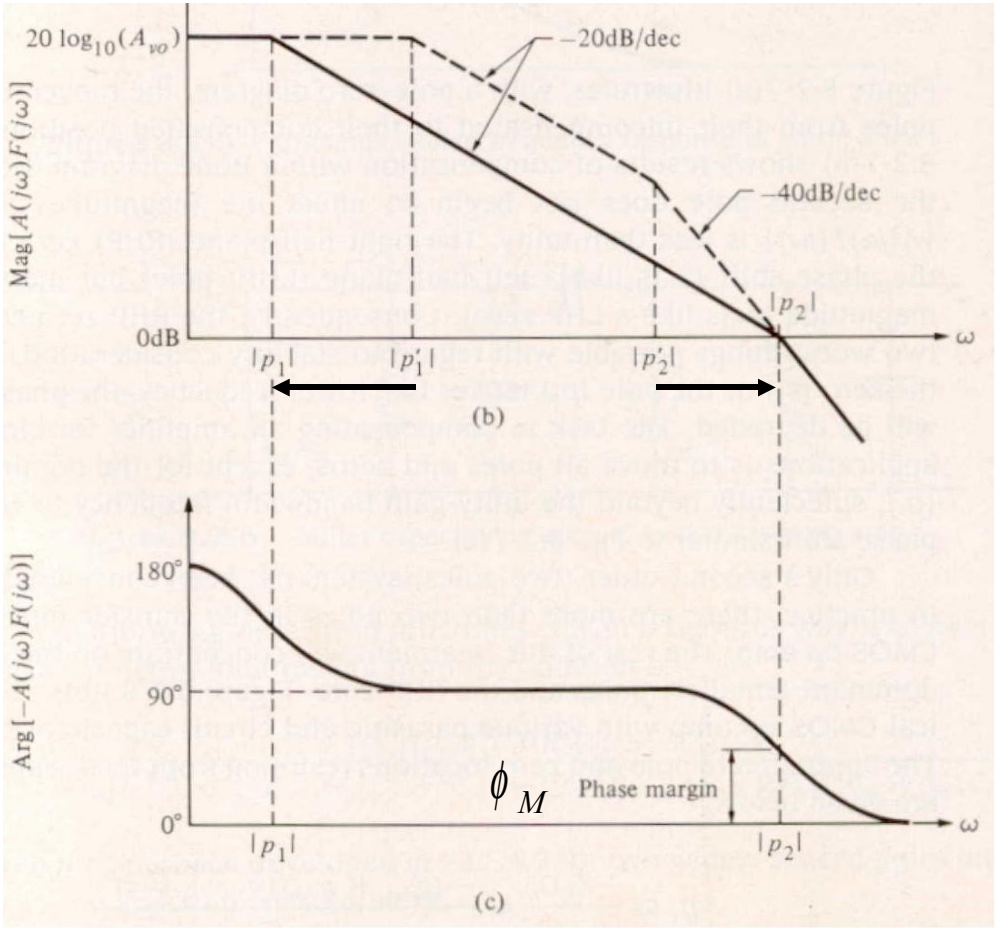
$$\frac{V_o}{V_{in}}(s) = \frac{A(s)}{1 + A(s)F(s)}$$

Allen & Holberg, 1st ed.

Amplificador Operacional de dois estágios
Resposta em freqüência

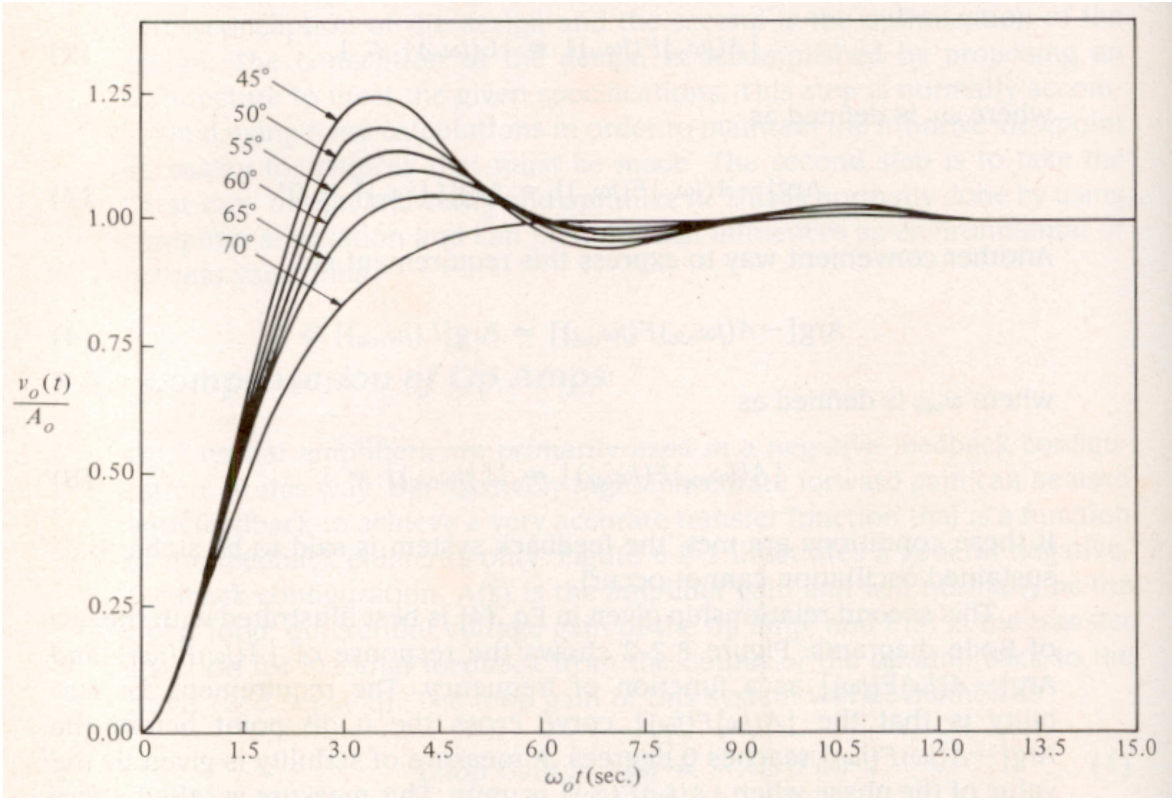


Allen & Holberg, 1st ed.



Amplificador Operacional de dois estágios

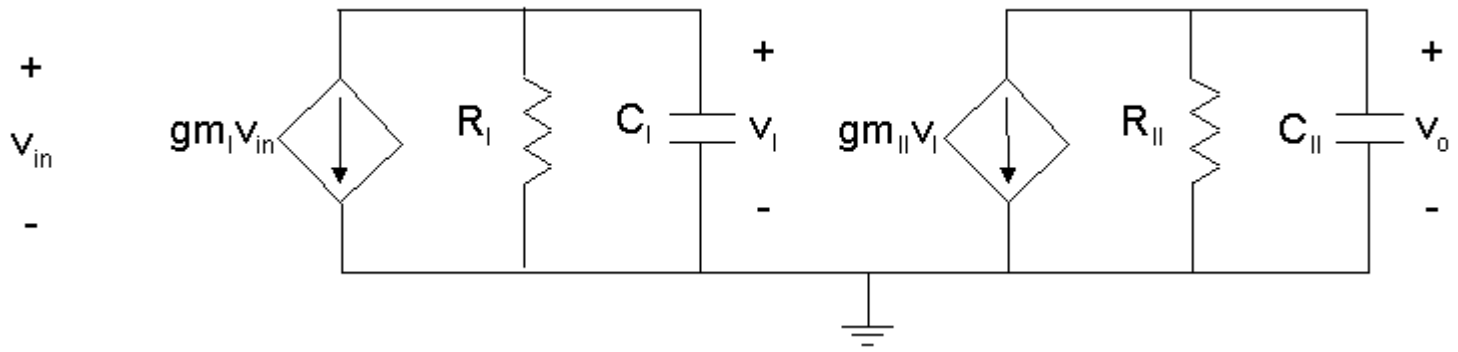
Resposta de um sistema de segunda ordem para vários valores de margem de fase



Allen & Holberg, 1st ed.

Amplificador Operacional de dois estágios não compensado

Circuito Equivalente diferencial



$$g_{mI} = g_{m1}$$

$$R_I = \left(g_{ds2} + g_{ds4} \right)^{-1}$$

$$C_I = C_{db2} + C_{db4} + C_{gb6} + C_{gs6}$$

$$g_{mII} = g_{m6}$$

$$R_{II} = \left(g_{ds6} + g_{ds7} \right)^{-1}$$

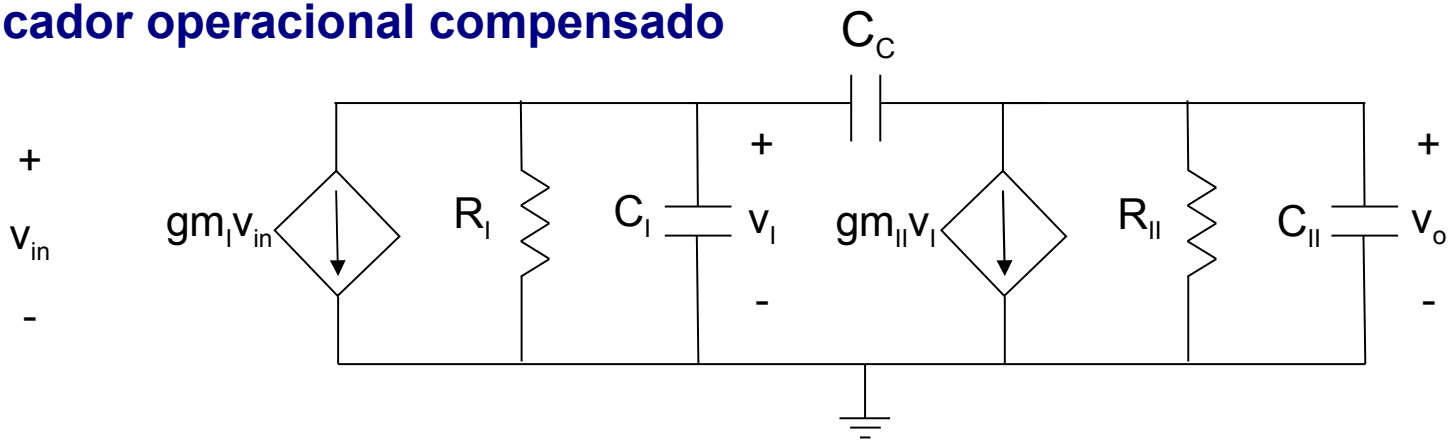
$$C_{II} = C_{db6} + C_{db7} + C_L$$

Se $C_C \rightarrow 0$, então

$$\frac{V_o}{V_{in}}(s) \cong - \frac{g_{mI} g_{mII} R_I R_{II}}{\left(1 + sR_I C_I\right)\left(1 + sR_{II} C_{II}\right)}$$

Pólos relativamente próximos, a margem de fase pode ser baixa ou até negativa!

Amplificador operacional compensado



$$A_d(s) = \frac{V_o}{V_{in}}(s) = -\frac{A_{d0}(1 - s/z)}{(1 - s/p_1)(1 - s/p_2)} \qquad A_{d0} = g_{mI} g_{mII} R_I R_{II}$$

$$p_1 \cong -\frac{1}{R_I(C_I + C_C) + R_{II}(C_{II} + C_C) + g_{mII} R_I R_{II} C_c} \cong -\frac{1}{g_{mII} R_I R_{II} C_c}$$

$$p_2 \cong -\frac{g_{mII} C_c}{C_I C_{II} + C_C(C_I + C_{II})} \cong -\frac{g_{mII}}{C_{II}}$$

$$z = \frac{g_{mII}}{C_c}$$

Nota: $2\pi\, GBW = A_{d0}|p_1| = g_{mI}/C_C$

$$SR = I_T / C_C$$

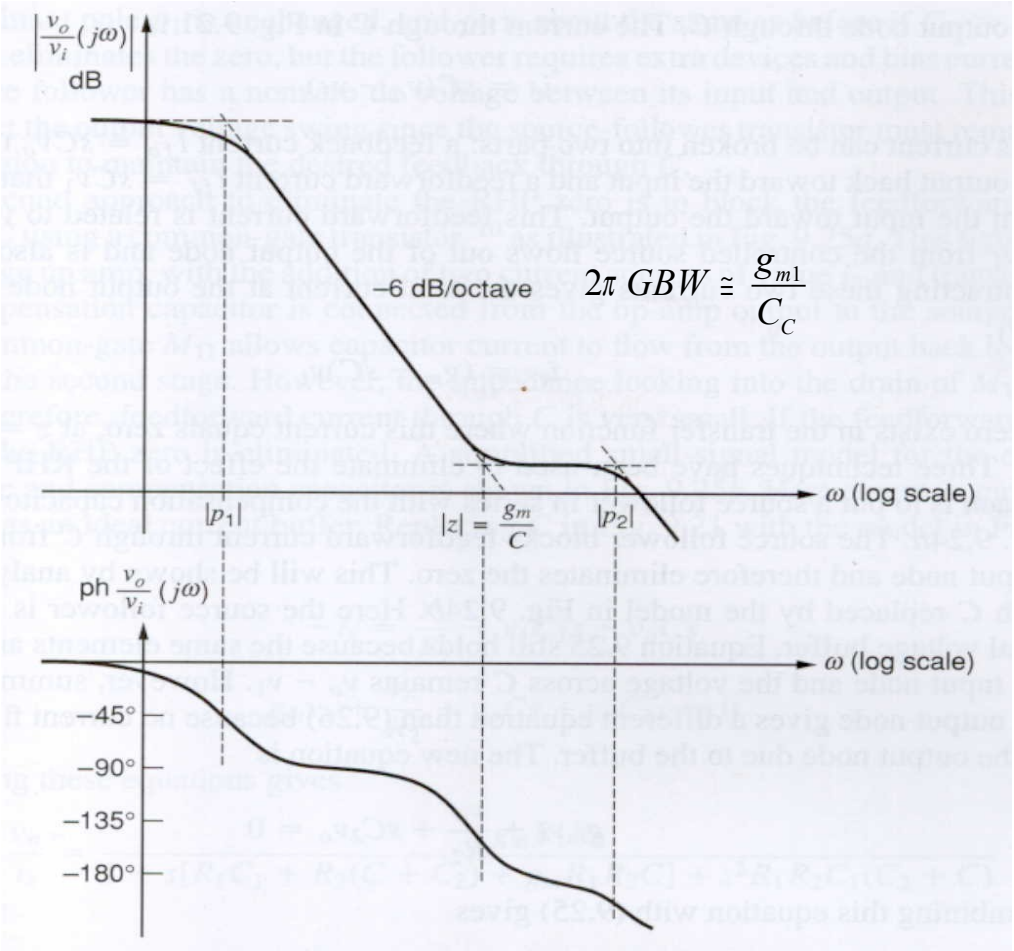
$$\frac{SR}{2\pi\, GBW} = (I_T / g_{mI}) = n\phi_t\left(\sqrt{1 + i_f} + 1\right)$$

Para evitar baixa margem de fase ,escolher

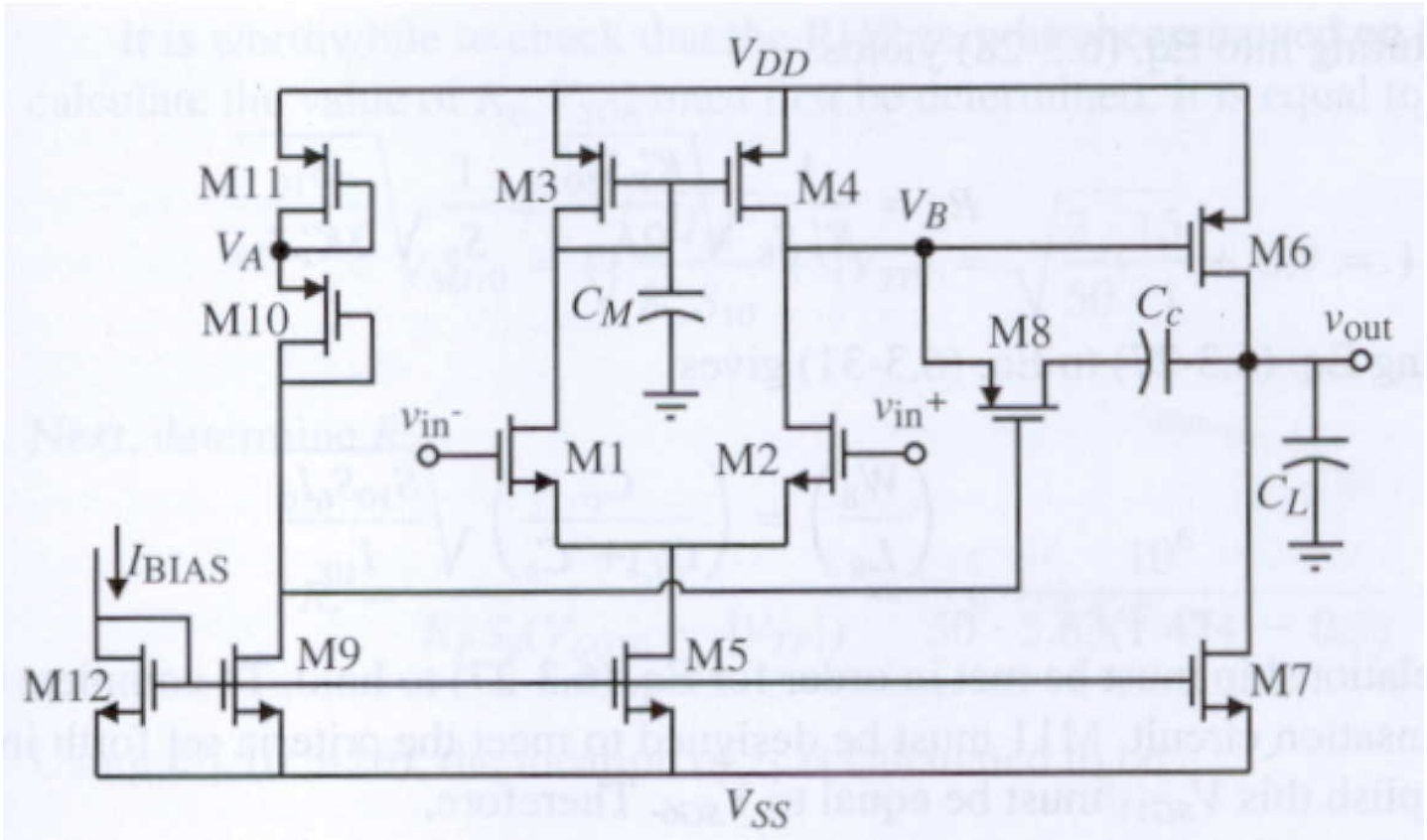
$$|p_2|, z > 2\pi\, GBW$$

$$\phi_M \cong \frac{\pi}{2} - \tan^{-1}\left(\frac{2\pi\, GBW}{-p_2}\right) - \tan^{-1}\left(\frac{2\pi\, GBW}{z}\right)$$

$$\left(\frac{g_{m1}(C_I C_{II}/C_C + C_I + C_{II})}{g_{m6} C_C}\right) \qquad \left(\frac{g_{m1}}{g_{m6}}\right)$$



Amp op CMOS de dois estágios com compensação RC



P. Allen and D. Holberg – CMOS Analog Circuit Design, 2nd. Ed., Oxford, New York, 2002.

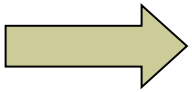
Amp op CMOS de dois estágios com compensação RC

$$p_1 \cong -\frac{1}{g_{mII} R_I R_{II} C_c}$$

$$p_2 \cong -\frac{g_{mII} C_c}{C_I C_{II} + C_C (C_I + C_{II})} \cong -\frac{g_{mII}}{C_{II}}$$

$$z = -\frac{1}{C_c (R_z - 1/g_{m6})}$$

$$p_3 = -\frac{1}{R_z C_I}$$

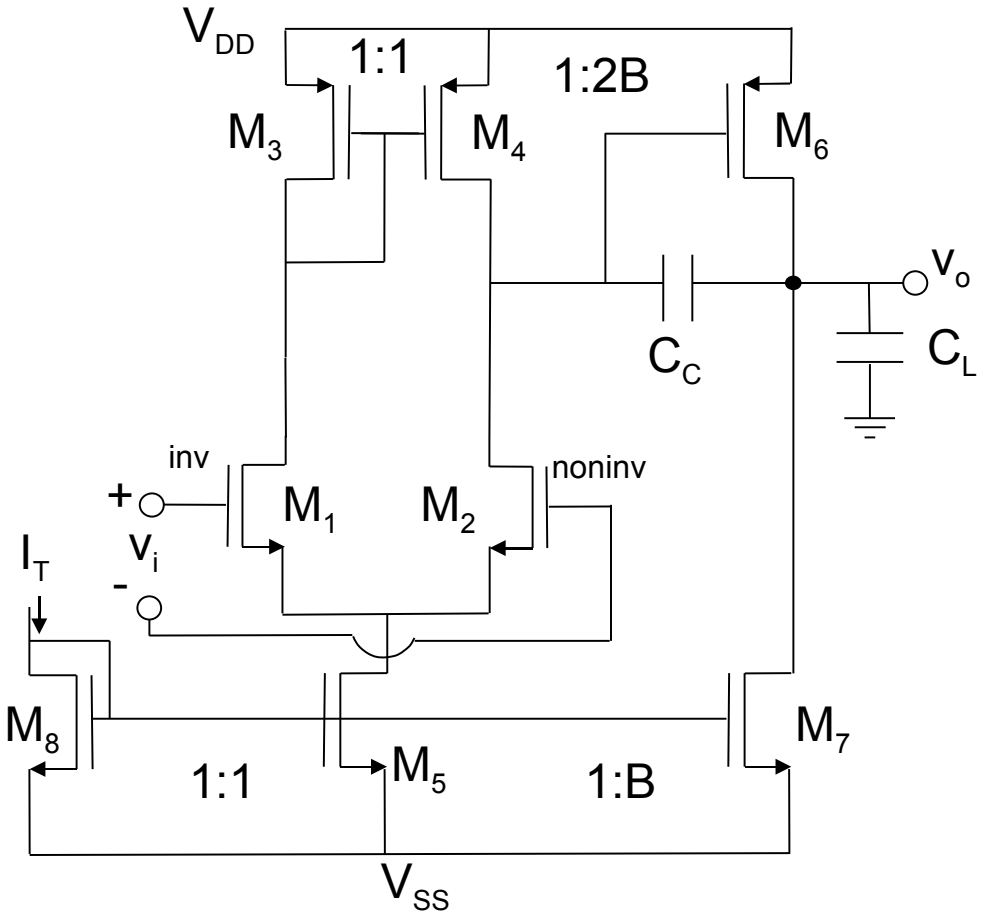


Pólo de alta freqüência

Colocando z sobre p_2: $R_z = \frac{1}{g_{m6}} \left(\frac{C_c + C_{II}}{C_c} \right) \cong \frac{1}{g_{m6}} \left(\frac{C_c + C_L}{C_c} \right)$

P. Allen and D. Holberg – CMOS Analog Circuit Design, 2nd. Ed., Oxford, New York, 2002.

Amplificador de dois estágios: equações de projeto



$$SR = I_T / C_C$$

$$2\pi\, GBW = A_{d0}\,|p_1| = g_{mI} / C_C$$

$$p_2 \cong -\frac{g_{mII} C_c}{C_I C_{II} + C_C\left(C_I + C_{II}\right)} \cong -\frac{g_{mII}}{C_{II}}$$

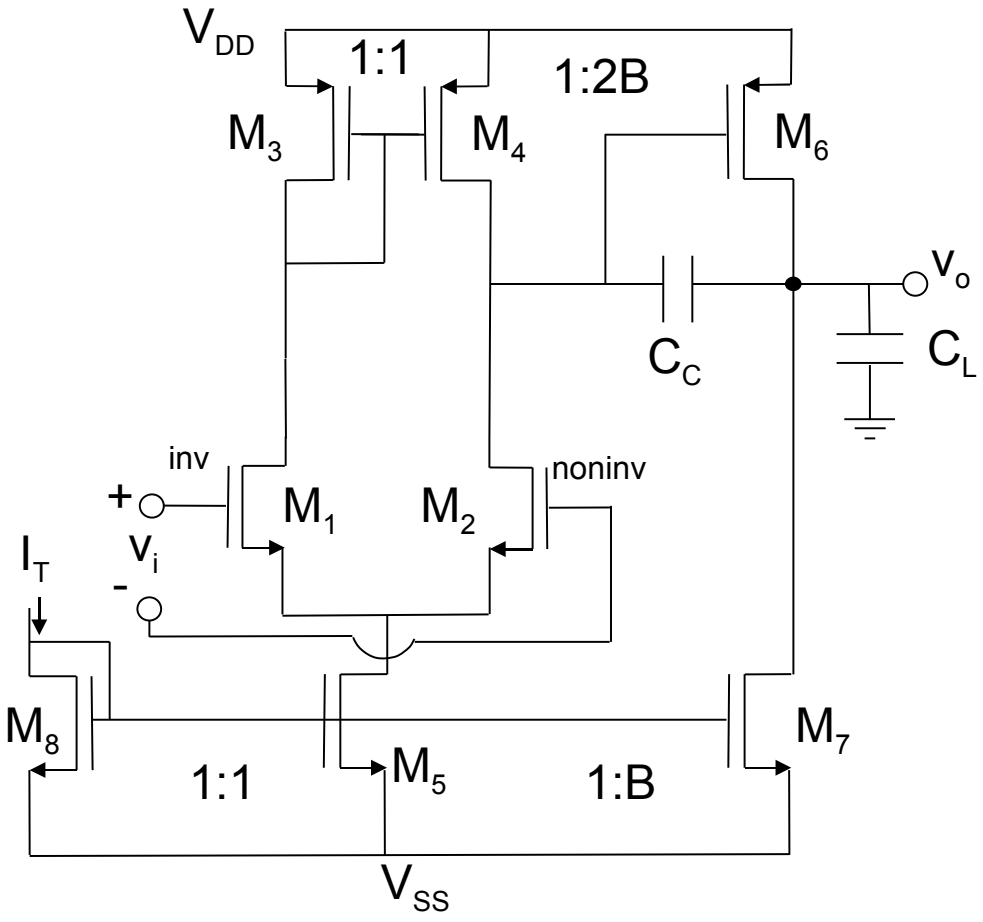
$$z = \frac{g_{mII}}{C_c}$$

$$A_{d0} = A_{d1} A_{d2}$$

$$A_{d1} = \frac{g_{m1}}{g_{ds2} + g_{ds4}}$$

$$A_{d2} = \frac{g_{m6}}{g_{ds6} + g_{ds7}}$$

Amplificador de dois estágios: equações de projeto



$$\left.\begin{aligned} V_{ICM\,\max} &= \\ V_{ICM\,\min} &= \end{aligned}\right\}$$ **Ver amp. dif.**

$$-V_{SS} + V_{DSsat7} < V_o < V_{DD} - \left|V_{DSsat7}\right|$$