Performance comparison between a multimode PA and a PA with adaptive biasing

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Abstract—*This work presents a schematic level 2.45 GHz power amplifier (PA) using multimode architecture in a 130 nm CMOS process. The amplifier is composed by three parallel differential cascode cells, which can be enabled or disabled by external bias voltages. With this configuration, the multimode PA has four operation modes. The high power mode presents a 12.2 dB small-signal gain, a 25.1 dBm output 1-dB compression point (OCP_{1dB}) and a 15.7% power-added efficiency (PAE). To optimize the multimode PA, removing the need for external digital circuits to select the operation modes, the same PA was tested using adaptive biasing. The new circuit provides an increasing bias voltage when input power reaches a certain threshold, changing the operation automatically. In this adaptive configuration, the PA presents a 9.3 dB small-signal gain, a 26.0 dBm OCP_{1dB} and a 26.9% PAE, improving both efficiency and linearity from the multimode amplifier.*

I. INTRODUCTION

In recent years, there has been a big increase on the number of telecommunications devices around the world. With this surge, the main concern around these devices is its efficiency and lifetime. Usually, the power supply for these devices is a battery, which has a life cycle (number of battery recharges) that defines when the devices stop working. To improve the lifetime of these devices, the efficiency of the circuits must be improved.

The power amplifier (PA) is one of the most consuming circuits on telecommunications devices [1]. A lot of techniques are studied to improve the efficiency of a PA, since it has a big impact on the overall efficiency of the device. For this purpose, a multimode PA can be used. In this architecture, different operation modes can be achieved changing the bias voltage. It Is possible to change the mode accordingly to the circuit's load to improve efficiency at power backoff.

Some examples of multimode PA can be seen in the literature. Santos *et. al.* presents the design for a two-stage power amplifier with a variable power stage, with seven unique operation modes [2]. Tarui *et al.* presents the design for a two-stage power amplifier, with variable power stage and gain stage, resulting in a six-mode PA [3]. Lastly, Luong *et. al.* presents a multimode and broadband PA, with four parallel unit power cells which can be enabled or disabled to achieve four different operation modes [4].

However, these circuits all share a common problem: the necessity of an external digital circuit to change between modes, adding a new degree of complexity to the device's project. To solve this problem, the adaptive biasing technique can be used. This technique works around circuits which can provide a rising bias voltage as the input power reaches a certain threshold point, changing the modes of a multimode PA automatically. Examples of adaptive biasing are seen in [5-6].

This paper presents a comparison between a multimode PA and a PA with adaptive biasing, using the same PA core in both cases. Firstly, a four-mode PA is tested, where mode selection is achieved through external bias voltages, changing the gain, output 1-dB compression point (OCP_{1dB}) and power consumption of the amplifier. In the second case, the external bias voltages are replaced by adaptive bias cells, whose function is to adaptively bias the cascode cells' transistor according to the input power. Sections II and III presents he design of the multimode power amplifier and of the adaptive bias cell, respectively. Section IV presents the results achieved through simulations.

II. MULTIMODE POWER AMPLIFIER

To achieve a wide output power range, a four-mode programmable PA is presented. The schematic of the amplifier's unit power cells is presented in Fig. 1. The circuit supply is a 3.1 V voltage. The amplifier is composed by three differential cascode cells, formed by 240 nm thick oxide transistors. The amplifier also has an RC feedback network to improve stability, composed of a 739 fF capacitor and a 390 Ω resistor, and an output matching network formed by a high pass LC configuration, composed of two 3.21 pF capacitors and a 3.26 nH inductor. Internal voltage reference circuits are used for transistor bias, providing a voltage of 1.17 V.

All capacitors in this circuit are dual-dielectric metal-insulator-metal (MIM). All the inductors have a central tap connection, which can be used to reduce the number of
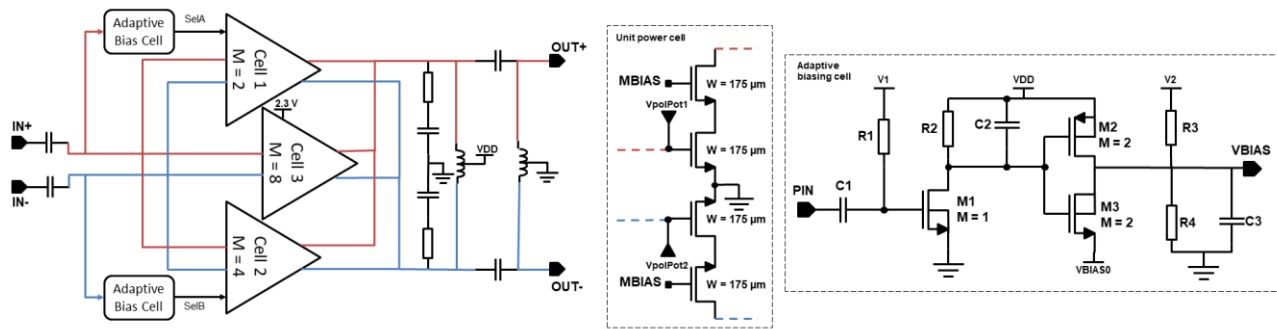
Fig. 1. *Block diagram showing all the connections of the proposed amplifier. In detail, the PA's unit power cell and the adaptive biasing cell schematic.*

inductors by half, reducing the occupied area in the layout. This change can be made since we designed a differential amplifier, with all the component values being symmetrical.

The unit channel width for all the transistors is 175 μm, with the difference between cells being the transistors' multiplicity. For the multimode configuration, the cells are turned off (0 V bias voltage) or on (2.3 V bias voltage) through the M_{BIAS} voltage, with external sources substituting the adaptive bias cells from Fig. 1. Turning the cells on or off changes the effective channel width of the circuit, varying between 350 μm and 2450 μm. For each width, a unique value of gain and OCP_{1dB} is achieved.

With three cells, the circuit has seven possible operation modes. However, for the modes where cell three is off, the amplifier presents poor gain (< 6 dB). So, in this design cell three is always on, and the four operation modes are achieved by turning cells one and two on or off.

III. ADAPTIVE BIASING

A. Schematic

Fig. 1 presents the schematic of the adaptive bias cell, based on the architecture proposed by Koo *et. al.* [6]. The threshold point of this circuit is defined by V_1 and the transistors' widths. For low input powers, M1 does not conduct, and V_{BIAS} assumes the value of V_{BIAS0}. When the input power rises past the threshold, M1 conducts, decreasing the gate voltage of M2. With this, M2 charges the V_{BIAS} node until the maximum output voltage.

M3 is used to achieve a faster discharge time for this cell. The body-drain connection creates a p-n junction diode between the body and source of the transistor, creating a new discharge path for the current flowing from M_2. Note that V_2 is not the maximum output voltage, as this supply only controls V_{BIAS} to a certain degree. So, V_{BIAS} can assume higher voltages than V_2. Two different adaptive bias cells are used, controlling both cell one and cell two from the PA. The components values and bias voltages for each cell are detailed in Table 1.

B. Design methodology

The input power threshold of the SelA adaptive bias cell was defined by the input refereed 1 dB compression point (ICP_{1dB}) of the multimode PA in the low power mode. With this, when the gain from the low power mode would start decreasing, SelA activates, maintaining the gain constant and improving the linearity of the PA. The same method was used for the threshold of the SelB adaptive bias cell, but with SelA already implemented. Ideally, the output bias of these cells should vary between 0 V to 2.3 V. However, the chosen architecture could not provide this voltage excursion. So, the multimode PA was further studied, identifying bias voltages different from 0 V while providing a similar gain. The chosen voltages were 1.2 V for SelA and 1.4 V for SelB.

As shown in the block diagram of Fig. 1, the adaptive bias cells are connected to different nodes of the differential input to maintain balance between the two nodes of the differential source, without overloading one of the sides, causing distortion to the input signal and, thereafter, to the output signal as well.

TABLE 1. VALUES OF THE ADAPTIVE BIAS CELLS

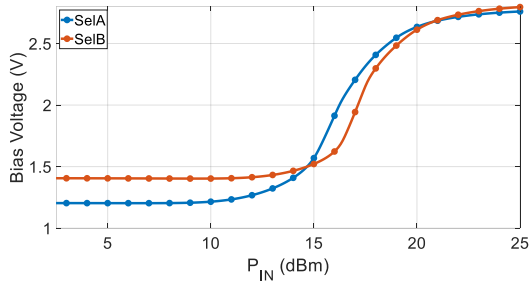|		SelA	SelB
Components	R1	60 kΩ	
	R2	1.91 kΩ	
	R3	2 kΩ	4 kΩ
	R4	6.3 kΩ	
	C1	1 pF	
	C2	10 pF	
	C3	10 pF	
	M1	W = 5 μm	W = 3.9 μm
	M2	W = 10 μm	
	M3	W = 10 μm	
Voltages	V1	0.5 V	
	V2	2.3 V	
	VBIAS0	1.2 V	1.4 V

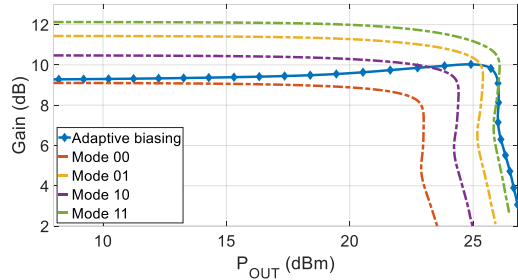Fig. 2. *Adaptive bias cell output voltage versus input power*

Fig. 3. *PA gain comparison between the multimode PA and a PA with adaptive biasing*

IV. SIMULATION RESULTS

The results were obtained using harmonic balance simulations with the Cadence Spectre RF simulator. To achieve these results, the input power varied between – 5 dBm and 25 dBm.

Tests were made to characterize all four operation modes of the multimode PA, followed by tests using the adaptive bias cell with the new output matching network. The four modes are described as binary words, representing the state of cells one and two of the amplifier, with 0 representing the cell turned off and 1 representing the cell turned on. The objective is to compare the results of the multimode PA and the PA with adaptive bias

Fig. 2 shows both SelA and SelB voltage versus the input power. For SelA, the output voltage varies between 1.2 V to 2.76 V and, for SelB, it varies between 2.79 V. Notice that the voltage used to put cells one and two on its on state is 2.3 V. Since the switching from the minimum to the maximum voltage in the adaptive bias cells is not abrupt, if the high value was 2.3 V, the amplifier would already have a 1 dB compression until the output voltage reached 2.3 V. So, a higher maximum output voltage was chosen, which also improves the linearity of the PA. Lastly, the difference between the threshold input power of both cells can be seen in the graph.

Fig. 3 shows the amplifier gain for the four modes of the multimode PA and for the PA with adaptive biasing versus the output power. A gain expansion can be seen for the adaptive biasing configuration. This happens since the bias voltage for low input powers is not 0 V. The cells were carefully designed so this gain expansion would not surpass 1 dB for both cases.
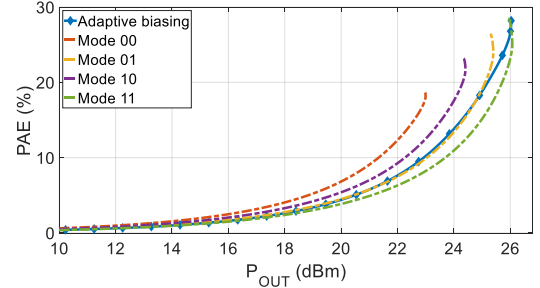

Fig. 4. *PAE comparison between the multimode PA and a PA with adaptive biasing*

TABLE 2. COMPARISON BETWEEN THE DIFFERENT TECHNIQUES

Operation mode	OCP_{1dB} (dBm)	Gain (dB)	PAE @ OCP_{1dB} (%)	Peak PAE (%)
00	22.8	9.1	16.3	18.6
01	24.9	11.4	18.1	26.4
10	24.1	10.5	18.5	23.1
11	25.1	12.2	15.7	28.5
Adaptive biasing	26.0	9.3 / 10.0[1]	26.9	28.2

[1] Peak value

For low input powers, the adaptive biasing mode has a similar behavior to the low power mode (00). As input power rises, the adaptive bias cells activate as shown in Fig. 2, maintaining an almost constant gain while improving the linearity. The gain for the PA with adaptive biasing starts decreasing for the same output power values when the high power mode (11) gain starts decreasing, showing that the new amplifier worked as intended.

Fig. 4 shows the amplifier power added efficiency (PAE) for the four modes of the multimode PA and for the PA with adaptive biasing. The adaptive biasing PAE shows an improvement over the high power mode PAE for every output power value, with the major improvement being 3.75 p.p. for a 25.32 dBm output power.

Table 2 detail the values of OCP_{1dB}, Gain and PAE for all the tests. The amplifier using adaptive biasing presents an OCP_{1dB} and PAE from all the tests, showing the best design for a wide output power range in terms of efficiency and linearity. Notice that with the adaptive biasing, a higher OCP_{1dB} than the high power mode was obtained, while consuming less power.

Table 3 depicts the performance comparison between this work and other PAs from the literature that utilize adaptive biasing. This work presents the best OCP_{1dB}, which is reasonable since it is the only differential amplifier. The gain could be improved by adding a gain stage in the input of the presented PA and the PAE could be improved implementing a multimode Doherty PA (as used by Chen *et. al* [6]).

TABLE 3. COMPARISON WITH THE LITERATURE

Ref.	Tech. Node (nm)	OCP_{1dB} (dBm)	Gain (dB)	PAE @ OCP_{1dB} (%)
[7]	180	21.4	10.6	33.0
[8][1]	180	23.0	24.6	17.0
[9]	180	21.8	14.0	30.4
This work[1]	130	26.0	9.3 / 10.0[2]	26.9

[1] Simulated results. [2] Peak value

V. CONCLUSION

A 2.45 GHz power amplifier using adaptive biasing in the 130 nm CMOS process was presented. The final circuit provided a 9.3 small-signal gain, a 26.0 dBm OCP_{1dB} and a 26.9% PAE. Using adaptive bias cells, the amplifier can change between the operation modes of the original structure without additional external circuits, while also improving both efficiency and linearity compared to the original amplifier for high output power values, with emphasis on the PAE which saw a 11.2 p.p. improvement @OCP_{1dB} and a similar value for peak PAE. However, for low output power values, the multimode PA shows a better efficiency in the correct operation mode.

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