Simulation Assessment of Cylindrical Vertical FETs Devices

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Abstract*— A pure silicon-based cylindrical vertical FET devices will be investigated through three-dimensional (3-D) numerical simulations. The Drain current (I_D) and transconductance (g_m) will be analyzed as a function of V_G (Gate voltage) for different channel length (L). The gate's length minimum value was 40 nm and the maximum gate's length was 120 nm (the maximum value of I_D = 65μA occurred for a channel length equal to 120 nm). Furthermore, the Threshold Voltage is analyzed. The results indicate that these structures are extremely competitive candidates for analog applications.

I. INTRODUCTION

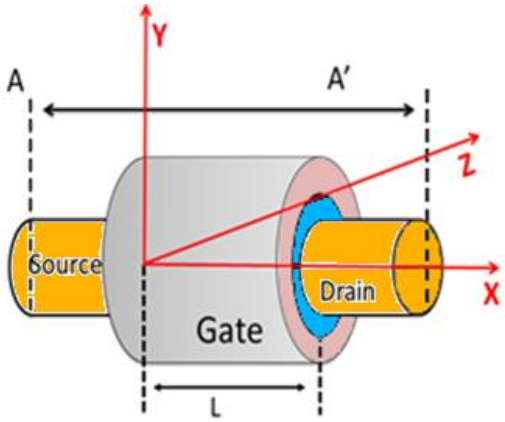
Cylindrical vertical FET transistors are still one of the mainly strategies being developed by MOS semiconductor manufacturers to create ever-smaller microprocessors and memory cells, referred to as extending Moore's law [1]. Many papers' have been published on the performance, operation, modelling and processing issues of such multigate-FET structures (FinFET and nanowire), but few analyze the effects that have occurred on this device, when one vary the length of Gate All Around, [2] for a device of total length 140 nm.

The cylindrical vertical FET devices are attractive candidates for sub-10 nm Non-Volatile Memories because the cylindrical geometry with a gate all around boosts the program and erases performances and also due to its advantage of 3D vertical stacking [3-6]. In this paper, we used the 3-D numerical simulator to investigate the transconductance and the threshold voltage.

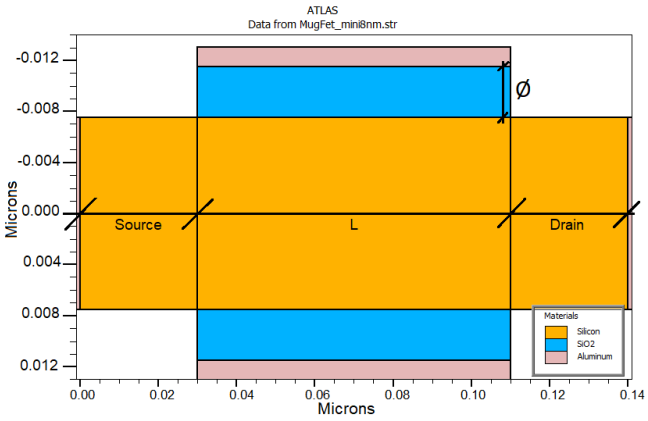
II. DEVICE DETAILS

In order to calibrate the simulations some important parameters such as: mobility, doping, models, and materials statements were setting in simulation. In the simulations, the appropriate physical mechanism models are including, such as the inversion layer mobility models Lombardi (Constant Voltage and Temperature - CVT), along with Shockley Read Hall (SRH) and Auger recombination models [7].

The model developed in the Atlas was adjusted to present electrical behavior similar to a real device whose characteristics were electrical measured at IMEC (Interuniversity Microelectronics Center) in Leuven (Belgium). A cross-sectional schematic of the Cylindrical Vertical FETs Devices used for the numerical simulations is illustrated in Fig. 1. The simulations were conducted with various gate lengths (40 nm, 60 nm, 80 nm, 100 nm, 120 nm).



(a)



(b)

Fig.1. *Schematic view of a Cylindrical Vertical device (a) and its schematic representation of the cross section along the channel A-A´ (b).*

Numerical simulations were conducted using the Silvaco ATLAS simulator [7] to verify our proposed methods. A hhi (Hot Hole Injection), hei (Hot Electron Injection), bbt.kane (Kane Band-To-Band Tunnelling Model), cvt (Lombardi (CVT) Model), srh (Shockley-Read-Hall), auger , bgn (Bandgap Narrowing) and print models [3] were included in the simulation. In addition, the solve method, with gradual gate polarization was used till the drain voltage reached 500 mV.

The drain current was successfully increased, in proportion to the increase in the gate length within the limits of the 140 nm device. On the other hand, gm (transconductance) and V_{TH} (threshold voltage) reached their maximum value around $V_G = 0.5$ V respectively.

The characteristics of the dispositive are:

- (L) Channel length - 40 nm
- Body diameter - 15 nm
- Drain length - 50 nm
- Source length - 50 nm
- (ϕ) Oxide thickness - 4 nm
- Doping of the drain and source - 10^{20} cm^{-3}, type N
- Doping of the body 10^{16} cm^{-3}, type P.

For each of the lengths, two graphs were drawn; [I_D x V_G] transconductance [gm x V_G] and threshold voltage was determinate [V_{TH}], as specified in Table I.

TABLE I. Threshold Voltage as a function of channel length.

Channel Length (L) (nm)	Threshold Voltage (V_{TH}) (µV)
120	58.6
100	59.2
80	59.6
60	59.9
40	64.2

The physical dimensions length and diameter, of the device were kept unchanged. The drain and the source were uniformly doped with n-type dopants 10^{20} cm^{-3} and the channel was uniformly doped with p-type dopants 10^{16} cm^{-3}.

III. PHYSICS-BASED SIMULATION

In order to make it possible to carry out the numerical simulations, first the structure was built up in a virtual environment.

The characteristic measures of the structures created, used to investigate the relationship between the gate length and drain current (I_D) are shown in Fig. 2.

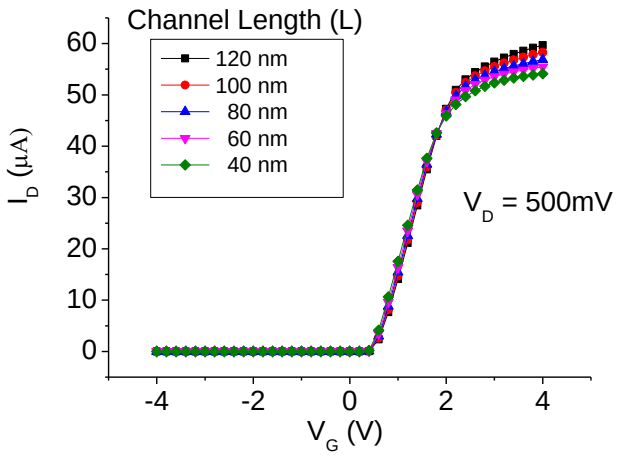


Fig .2. *I_D x V_G curves for different channel lengths.*

The graph in Fig. 2 shows the response of drain current (I_D) as a function of gate voltage (V_G). We found that for $V_G < 2$ V, the response curve was coincidence, for each analyzed device. For $V_G > 2$ V, the highest I_D current value (65 µA) was verified for the device with the longest channel length (120 nm). Finally, we found the lowest I_D value (48 µA) for the device with shortest channel length (40 nm).

After analyzing the I_D x V_G curves in Fig. 2, another point of interest was analyzed, the transconductance. Transconductance is a quantity that basically shows how much the gate voltage is effective in controlling the drain current, a parameter that is essentially in the analysis of devices on nanometric scales [8].

To perform this analysis, the graphs previously produced (I_D x V_G) and the first derivatives of these were performed, in order to validate the transconductance values, the results obtained are shown in Fig. 3.

The transconductance's graph as a function of gate' voltage (V_G), on the other hand, presented a more concise result, as the curves were practically coincident, regardless of the length of the channel.

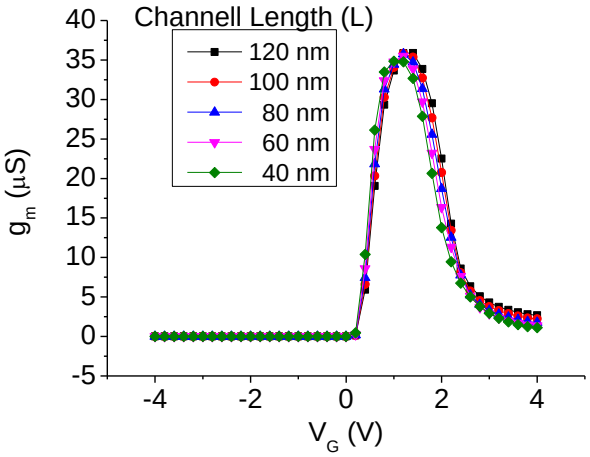


Fig. 3. *Transconductance (g_m) as a function of channel length (L) for V_D = 500mV.*

With the transconductance graphs it is also possible to obtain the values of threshold voltage through the derivative of the transconductance curve. According to [9], the threshold voltage is the voltage applied to the transistor gate, where the derivative of the transconductance has its maximum value.

IV. Conclusion

This work showed that 3-D numerical simulations can replicate the behavior of Cylindrical Vertical FETs Devices. The drain current flow was proportional to the voltage applied to the gate. The highest drain current value, (I_D = 60 µA), occurred when the gate length was 120nm. Transconductance showed its greatest value (gm = 35 µS) when the gate length was 40 nm. And the highest threshold voltage value (V_{TH} = 64 µV) also occurred for the gate with a length equal to 40 nm.

Acknowledgments

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