AN INVESTIGATION ON THE GATE PULSE PATTERN FOR THE 'KURII' RECTIFIER

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Abstract **- The 'Kurii' rectifier is a three-phase AC to DC converter that achieves high power factor and low THD in the input current, employing three bi-directional switches on a diode bridge. This work describes the results of extensive circuit simulation to evaluate the role of different gate pulse patterns on the circuit's power factor and output voltage. As a result, several graphs of the power factor characteristic were produced, showing the best gate pulse scheme for a particular application. It was resolved that, for variable load conditions, short gate pulses achieve best results than the 30° pulses used on previous works. Some experimental data, acquired from a 7.3 kW laboratory prototype, are also provided and validate the conclusions.**

I. INTRODUCTION

In the recent years a number of new circuits have been introduced for AC-to-DC high-power conversion, with high power factor and low THD in the input current. Among them, the 'Kurii' rectifier [1, 2, 3] shown in Figure 1 is a three-phase AC-to-DC converter that employs three low-power bi-directional switches in a conventional three-phase diode bridge with input inductors. The main features of the new circuit are low cost, small size, high efficiency and simplicity.

The switches' gate pattern employed in the converter plays an important role on the circuit's behavior. In [1], each of the three bi-directional switches is gated on when the respective phase voltage is null, with a fixed gate pulse width equivalent to $^1/_{12}$ of the voltage period, or 30°. As a result, the converter shows a power factor over 0.99 for a given load, with 6.1% for the THD in the input current. However, if the load of the converter is lower or higher than the nominal value, both the power factor and the THD are deteriorated.

The same circuit was also investigated in [4], with each of the bi-directional switches gated with high-frequency width-modulated pulses (PWM) during a 60° interval (30° before the zero-volt transition and 30° after the transition). With such gate pulse scheme, the input current shows a low THD over an extended power output range. The width-modulated pulses are however more complicated to be generated than the low-frequency pulses used in [1].

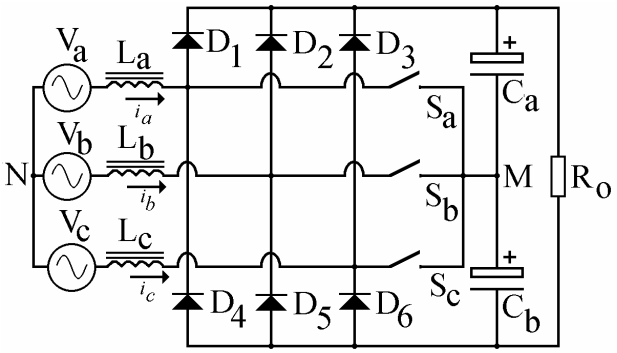

Figure 1: The 'Kurii' three-phase rectifier. $\mathbf{S_a}$, $\mathbf{S_b}$ and $\mathbf{S_c}$ are low-power bi-directional switches.

In [2] and [3], a low-frequency variable-width gate pulse pattern was used for the same circuit, showing that for low load levels the power factor can be increased with gate pulses equivalent to 25° or 20°. Nevertheless, the main interest in [2] and [3] was to use gate pulses with variable width to keep the output voltage of the converter on a constant value.

This paper presents an investigation on the role that the low-frequency gate pulse plays on the power factor of the 'Kurii' rectifier. The analysis was performed using extensive circuit simulation employing PSpice, with several load values and two different gate pulse patterns. The same gate schemes were implemented in two different gating circuits and used on a 7.3 kW laboratory prototype, showing similar behavior to the numerical simulation results.

II. DEVELOPMENT

A. Investigation on the Gate Pulse Relative Position

In [2] and [3] the gating pattern was that displayed in Figure 2.a, which can be called a "zero-started" gate pulse. In such scheme, the switch is gated on when the phase voltage is null and the gate pulse width (denoted by α) can be adjusted from zero to a maximum of 30°. An alternative scheme is in Figure 2.b, that is a "30°-terminated" one; the gate pulse width can be also adjusted from zero to 30°, but the switch is always gated off at 30°.

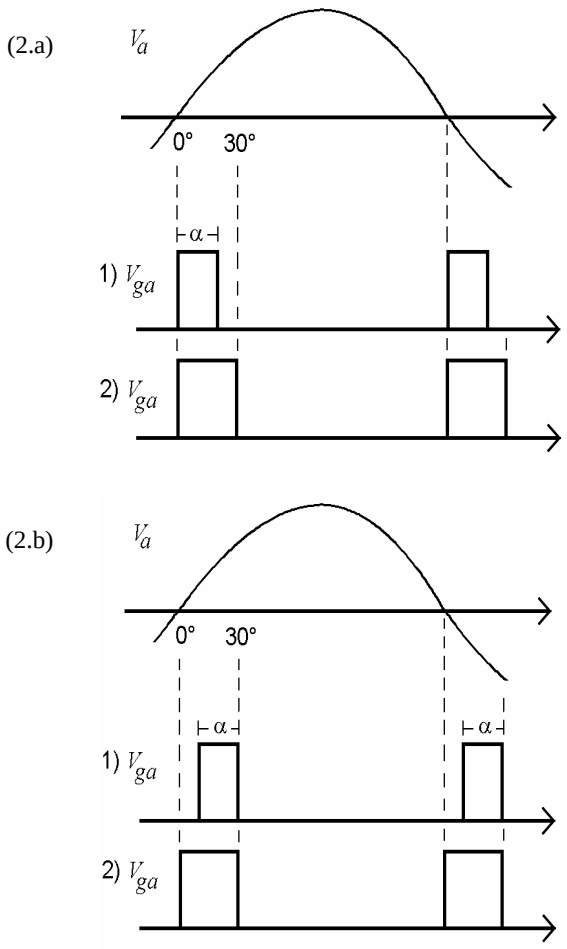

Figure 2: Two alternatives for the gate pulses with variable width: In (2.a), a "zero-started" pulse scheme, where the switch is gated on at the zero-voltage transition. In (2.b), it is showed the "30°-terminated" gate pulse pattern, where the switch is gated off at 30°.

Using gate pulses as shown in Figure 2.a, the current trough the corresponding bi-directional switch is shown in Figure 3.a (upper) for a simulation using $\alpha = 15°$ and resistive load of 11.2 Ω. Figure 3.b (down) is for a simulation of the same circuit, also with $\alpha = 15°$ and 11.2 Ω load, but employing the pulse scheme from Figure 2.b. Table I shows the numerical results for those simulations.

TABLE I

Simulation results of a 'Kurii' rectifier with 11.2 Ω load and two gate pulse schemes, both with α = 15°

Pulse Scheme	zero-started	30°-terminated
Output Power	5827.7 W	6979.6 W
Output Voltage	255.5 V	279.6 V
THD of Input Current	9.8 %	7.9 %
Displacement of Fundamental	32.2°	11.1°
Power Factor	0.842	0.975

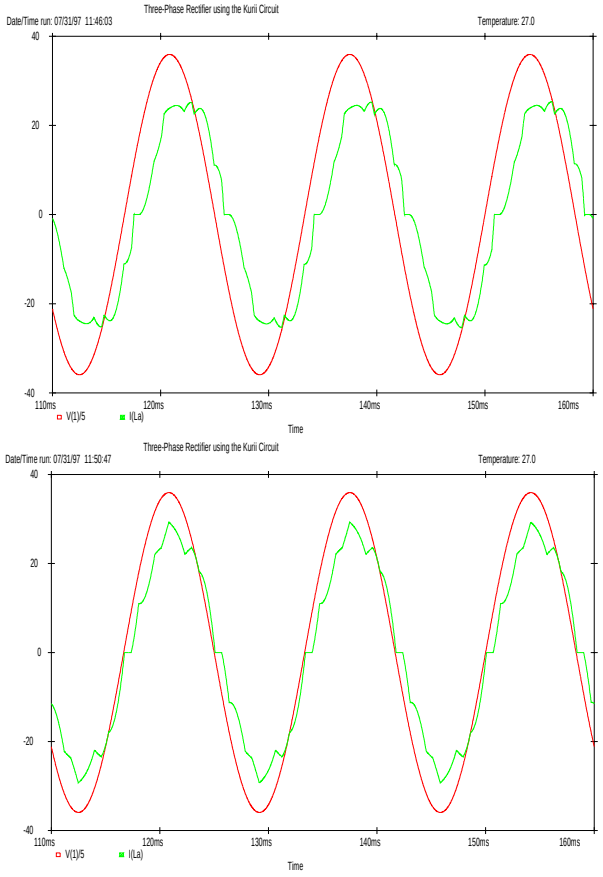

Figure 3: Input Current and phase voltage achieved by circuit simulation of a 'Kurii' rectifier; upper (Fig. 3.a), using "zero-started" gate pulses; and down (Fig. 3.b), employing "30° terminated" gate pulses, both with 11.2 Ω load and α = 15°.

It is manifest from the simulation results in Table I that the "30°-terminated" scheme gives a higher output voltage than the "zero-started" scheme for the same load resistance and pulse width. The power factor, however, must be compared for the same output power for both gate schemes. Figure 4 shows the result of a set of circuit simulation for a 7.3 kW 'Kurii' rectifier, using "zero-started" pulses and "30°-terminated" pulses, both with $\alpha = 15°$. The power factor for the "30°-terminated" scheme is significantly higher in a wide range than the power factor for the "zero-started" pattern. On the other hand, Figure 5 also shows that the output voltage is considerably higher for the "30° terminated" scheme.

B. Investigation on the Best Pulse Width

For a given load, one can calculate the "critical inductance" [2] for the 'Kurii' circuit employing Equation 1, where P is the DC power output of the rectifier and V is the peak value of the AC phase-to-neutral input voltage:

$$L = \frac{54 \cdot V^2}{7 \cdot \omega \cdot \pi^2 \cdot P}\left(2\sqrt{3} - 3\right) \qquad (1)$$

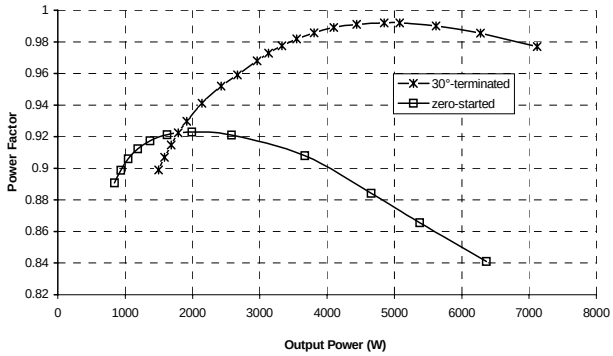

Figure 4: Power Factor of the 'Kurii' Rectifier for two gate pulse schemes with $\alpha = 15°$.

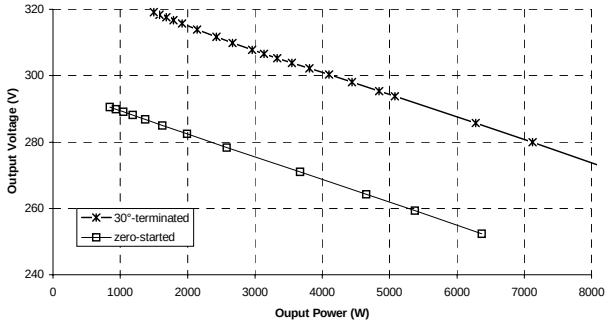

Figure 5: Output Voltage of the 'Kurii' Circuit for two gate pulse schemes with $\alpha = 15°$.

Using the appropriate critical inductance with $\alpha = 30°$ and nominal load condition, the converter operates on an optimized situation, the THD of the input current is about 6% and the resulting power factor is over 0.99. However, in practical applications it is quite normal that a rectifier operates with lower loads than the nominal value. For such situation, the choice of $\alpha = 30°$ is not convenient, because both the THD and power factor deteriorate with low load, as shown in Figure 6. As a result, a better pulse pattern must be chosen for converters that operate with variable load.

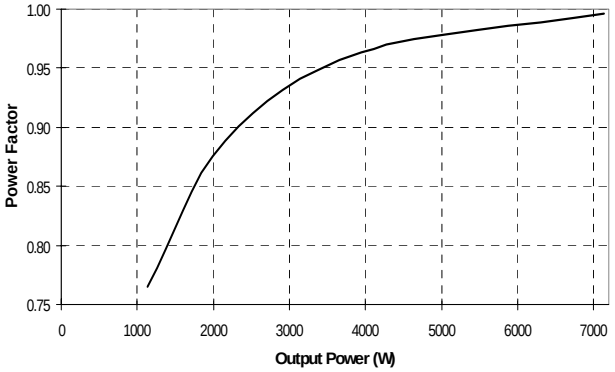

Figure 6: Power factor of a 'Kurii' rectifier using L = 4.2 mH and $\alpha = 30°$.

Using extensive circuit simulation with PSpice, Figure 7 was produced, showing the influence of the pulse width on the power factor of a 'Kurii' rectifier with 7.3 kW nominal output power and 220 V rms input line voltage. For such values, Equation 1 gives the "critical inductance" $L = 4.2$ mH, and the simulations were accomplished using the "30°-terminated" gate pulse scheme from Figure 2.b.

It can be seen in Figure 7 that the converter can operate on a wide load range with high power factor if a gate pulse other than 30° is adopted. For instance, if a power factor of 0.95 is considered high enough on a given application, it is better to have $\alpha = 10°$ than $\alpha = 30°$. It is evident that adopting $\alpha = 30°$, a power factor as high as 0.99 can be obtained, but the load must be kept nearby the nominal value.

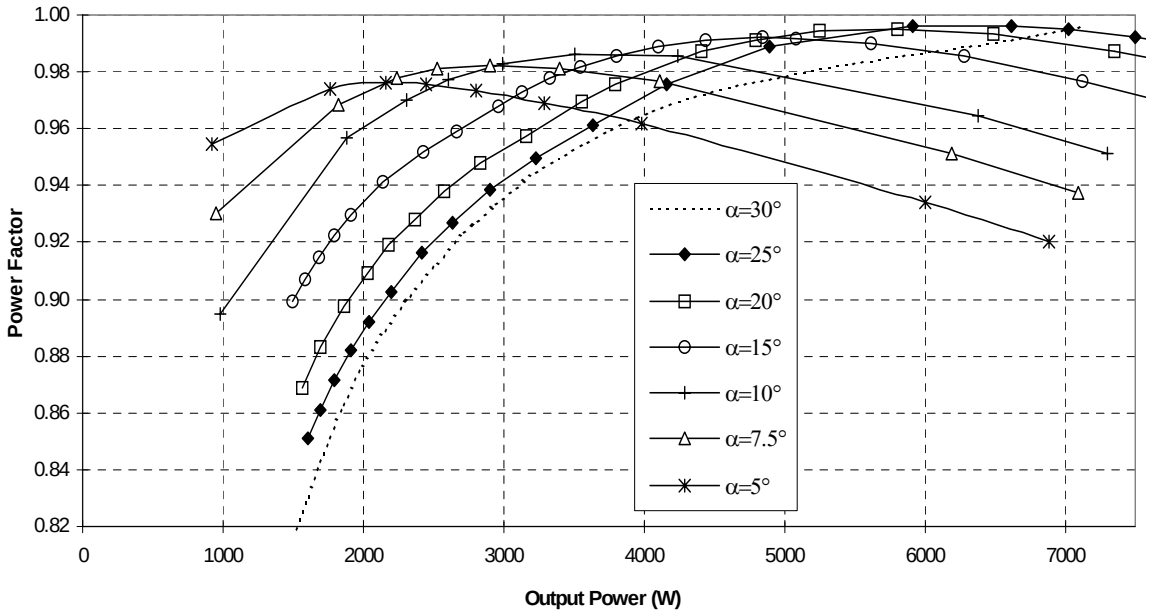

Figure 7: Power factor of a 'Kurii' rectifier with L = 4.2 mH and 220 V rms input line voltage, employing several gate pulse widths and the "30°-terminated" gating scheme from Figure 2.b.

C. Experimental Work

A laboratory prototype was assembled to validate the results from the simulations. Such prototype has its main characteristics as follows, and circuit diagram as in Figure 1:

- Input line voltage: V_i = 220 V, 60 Hz.
- Input inductors: $\mathbf{L_a} = \mathbf{L_b} = \mathbf{L_c}$ = 4.25 mH
- Rated output power: $\mathbf{P_o}$ = 7.3 kW

Each of the bi-directional switches $\mathbf{S_a}$, $\mathbf{S_b}$ and $\mathbf{S_c}$ was assembled with a IRF840 (International Rectifier) MOSFET (**M**) connected between the DC nodes of a rectifier bridge, made with four SK3/12 Semikron diodes ($\mathbf{D_a}$, $\mathbf{D_b}$, $\mathbf{D_c}$ and $\mathbf{D_d}$), as shown in Figure 8. Although no overvoltage stresses were observed, the switches' assembly leads to a small parasitic inductance, so a small "snubber" circuit (Figure 8) was also added to each switch ($\mathbf{D_s}$ is a 1N4007 diode, $\mathbf{R_s}$ is a 1.2 kΩ resistor and for $\mathbf{C_s}$ two 0.25 µF / 250 V in parallel were used).

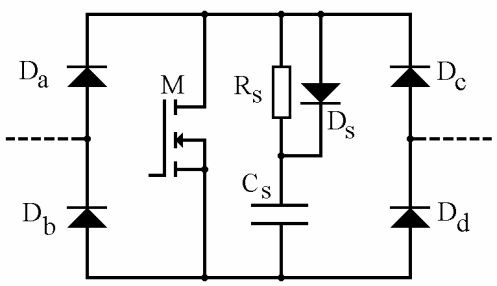

Figure 8: Circuit for each of the bi-directional switches $\mathbf{S_a}$, $\mathbf{S_b}$ and $\mathbf{S_c}$ used in the prototype.

The main rectifier diodes ($\mathbf{D_1}$ to $\mathbf{D_6}$ in Figure 1) were SKN21/02 Semikron, with heat sinks. The input inductors $\mathbf{L_a}$, $\mathbf{L_b}$ and $\mathbf{L_c}$ were constructed with ordinary silicon-steel *E-I* sheets, with air gap to provide inductance adjustment. For the output capacitors ($\mathbf{C_a}$ and $\mathbf{C_b}$ in Figure 1), four 2200 µF / 250 V Icotron series 87500 capacitors were used. Those capacitors withstand the additional pulses from the bi-directional switches.

For the experimental analysis of the "zero-started" gate scheme and the "30°-terminated" one, two different gate circuits were built. Both use three TCA785 IC for detecting the zero transition on the input voltage, but each has different logic circuits with CMOS ICs to produce gate pulses as shown in Figure 2.a and 2.b. Each of the gate circuit was assembled in separated printed-circuit boards, but with identical connections to the power circuit. As a result, the gate circuits could be easily changed to perform comparative tests. In each of the printed circuit boards, multi-turn trim-pots allow a precise adjustment on the pulse width.

Figure 9 shows the input current and the phase voltage for the prototype, with an 11.2 Ω resistive load, using the gate circuit with "zero-started" scheme. The same resistive load, but with the "30°-terminated" pattern, produced the results shown in Figure 10. The numerical values of the curves shown in Figures 9 and 10, obtained with a Tektronix TDS724A digital oscilloscope, were used in a numerical analysis program to perform the fast Fourier-transform to calculate the power factor and THD of the input current. Table II summarizes the numerical results of the tests shown in Figures 9 and 10, that are very similar with the simulated ones presented in Table I.

Other tests and measurements, for different load resistance and using the two gating circuits, also showed that the experimental behavior of the 7.3 kW prototype agrees in a high degree with the simulation results.

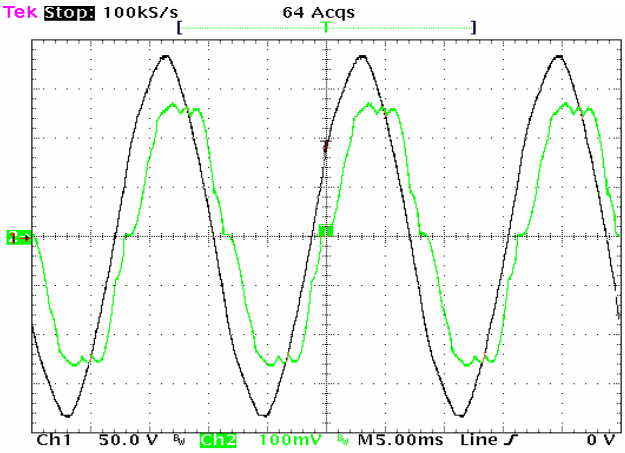

Figure 9: Input phase voltage and current for the prototype, using the "zero-started" gate pattern, α = 15° and 11,2 Ω load. Voltage scale: 50 V/div; current scale: 10 A/div (using a 10 mV/A Current Probe - Tektronix A622).

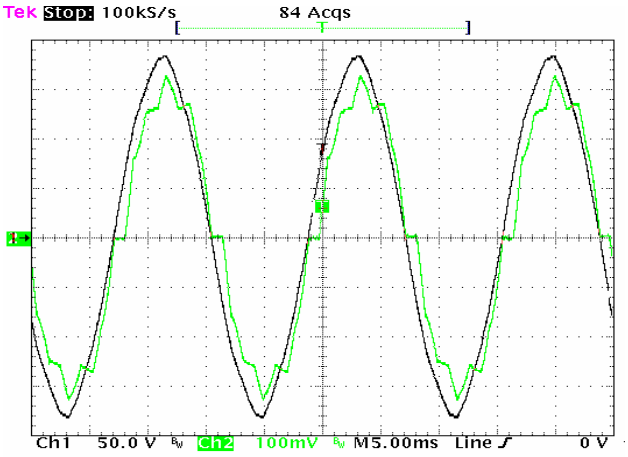

Figure 10: Input phase voltage and current for the prototype, using the "30°-terminated" gate pattern, α = 15° and 11,2 Ω load. Voltage scale: 50 V/div; current scale: 10 A/div (using a 10 mV/A Current Probe - Tektronix A622).

TABLE II

Experimental results of the prototype, with 11.2 Ω load and two gate pulse schemes, both with α = 15°.

Pulse Scheme	zero-started	30°-terminated
Output Power	5670.0 W	6900.4 W
Output Voltage	252 V	278 V
THD of Input Current	10.22 %	9.7 %
Displacement of Fundamental	28.9°	11.9°
Power Factor	0.870	0.973

III. CONCLUSIONS

An extensive investigation was conducted employing circuit simulation of the 'Kurii' circuit with different gate pulse patterns. Some conclusions were ensued:

- The simulations and experiments employing the "30°-terminated" gate scheme shows higher power factor than the "zero-started" one. The output voltage is also higher with the "30°-terminated" gate scheme than the voltage achieved with the "zero-started" pattern. As a result, the "30°-terminated" scheme must be used in future applications.

- If the converter is intended to be used with a fixed load or with loads of small variation, $\alpha = 30°$ must be adopted and the resulting power factor will be higher than 0.99, using the critical inductance for $\mathbf{L_a}$, $\mathbf{L_b}$ and $\mathbf{L_c}$.

- For a converter connected to a variable load, gate pulses with short width can be used. For example, if a power factor over 0.95 is acceptable, $\alpha = 10°$ may be used and thus the load can be varied from 20% to 100% of the nominal value.

- If a near-unity power factor is imperative over a wide load range, a far more complicated gate circuit must be designed, able to produce gate pulses with variable width as a function of the output current of the converter.

On the experimental work, both the "30°-terminated" gating circuit and the "zero-started" one were used on the same prototype, rated at 7.3 kW output power. The experimental results were very similar to the simulation ones, validating the conclusions.

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