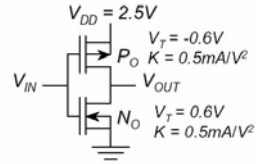
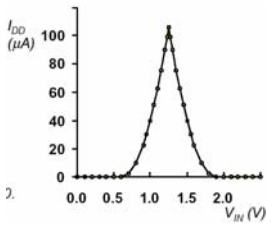
DC Current in CMOS

- For $V_{IN} < V_{TN}$, N_O is cut off and $I_{DD} = 0$.
- For $V_{TN} < V_{IN} < V_{DD}/2$, N_O is saturated.
- For $V_{DD}/2 < V_{IN} < V_{DD}+V_{TP}$, P_O is saturated.
- For $V_{IN} > V_{DD} + V_{TP}$, P_O is cut off and $I_{DD} = 0$.
- • For $V_{DD}/2 < V_{IN} < V_{DD}+V_{TP}$, PO is saturated.
- • For $V_{IN} > V_{DD} + V_{TP}$, PO is cut off and $I_{DD} = 0$.
- Even though CMOS exhibits negligible DC dissipation in either logic state, appreciable power is dissipated during switching.





Power dissipation in CMOS

- **Dynamic Power Consumption**

  Charging and Discharging Capacitors

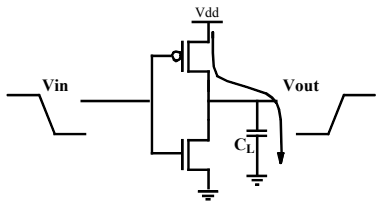
- **Short Circuit Currents**

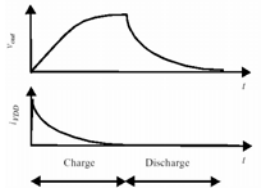
  Short Circuit Path between Supply Rails during Switching

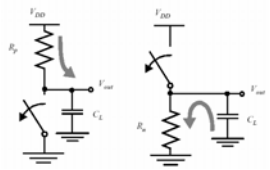
- **Leakage**

  Leaking diodes and transistors

Dynamic Power Dissipation







Capacitor Energy:

$E_C = 1/2\ C\ V_{dd}^2$

Dynamic Power Dissipation

For each transition (clock cycle):

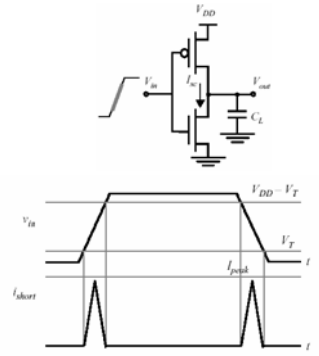
$$\text{Energy/transition} = C_L * V_{dd}^2$$

$$\text{Power} = \text{Energy/transition} * f = C_L * V_{dd}^2 * f$$

- **Not a function of transistor sizes**
- **Need to reduce C_L, V_{dd} and f to reduce power.**

Dissipation Due to Direct-Path Currents

- during switching the NMOS and the PMOS transistors are conducting simultaneously.
- This puts the power supply in "short-circuit" during the transitions of the input signal
- "short-circuit" current is limited by transistors current capacity ⇒ depends on transistor size

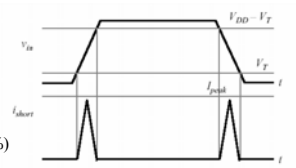


Dissipation Due to Direct-Path Currents

t_{sc}: shot circuit duration

$$t_{sc} = \frac{V_{DD} - 2V_T}{V_{DD}} t_s \approx \frac{V_{DD} - 2V_T}{V_{DD}} \times \frac{t_{r(f)}}{0.8}$$

$t_{r(f)}$: rise (fall) time of input signal (10%-90%)



$$E_{dp} = V_{DD}\frac{I_{peak}t_{sc}}{2} + V_{DD}\frac{I_{peak}t_{sc}}{2} = t_{sc}V_{DD}I_{peak}$$

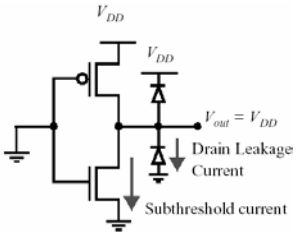
$$\boxed{P_{dp} = t_{sc}V_{DD}I_{peak}f}$$

I_{peak}: peak current of transistors ($Vo=V_{DD}/2$)

f: switching frequency

Dissipation Due to Leakage

- reverse-biased diode junctions and transistors leakage
- 10-100 pA/μm^2 at room temperature.
- Increases exponentially with temperature



$$P_{stat} = I_{stat}V_{DD}$$

I_{stat}: leakage currents

Total Power Dissipation

$$P_{tot} = P_{dyn} + P_{dp} + P_{stat}$$

$$P_{tot} = (C_L V_{DD}^2 + V_{DD}I_{peak}t_s)f_0 + V_{DD}I_{leak}$$

- *Low frequency operation: P_{stat} dominates*
- *High frequency operation: P_{dyn}+P_{dp} dominates*