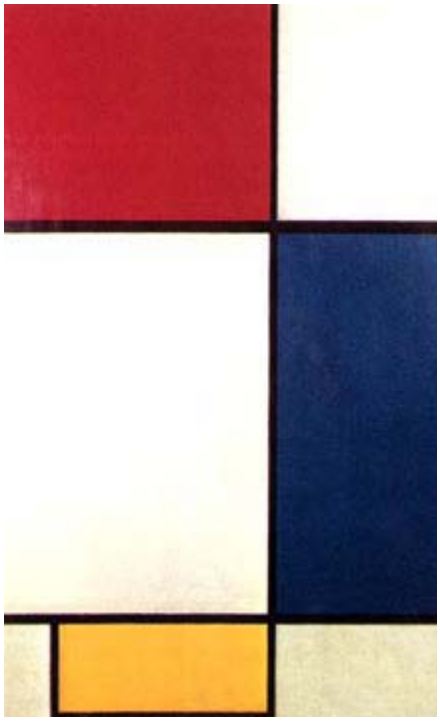
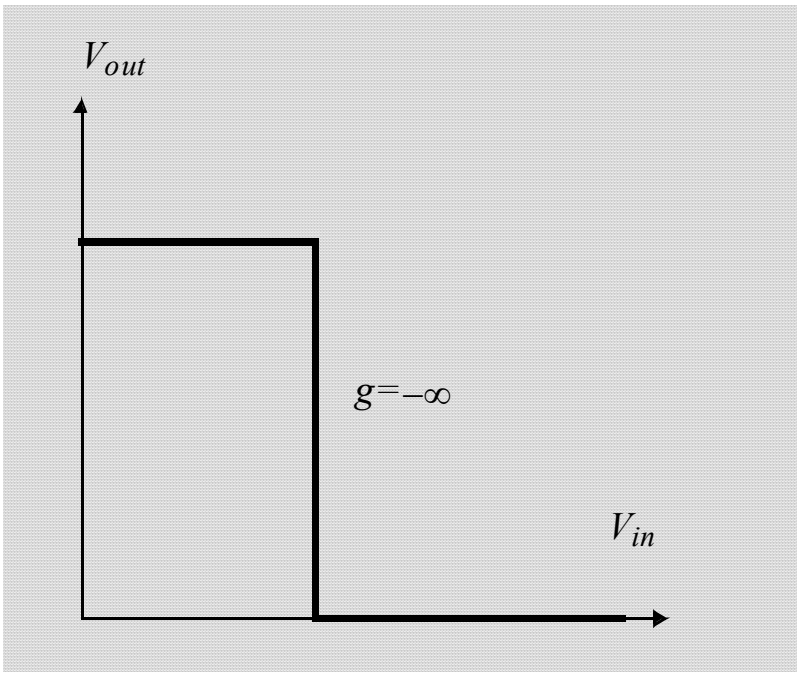
CMOS INVERTER



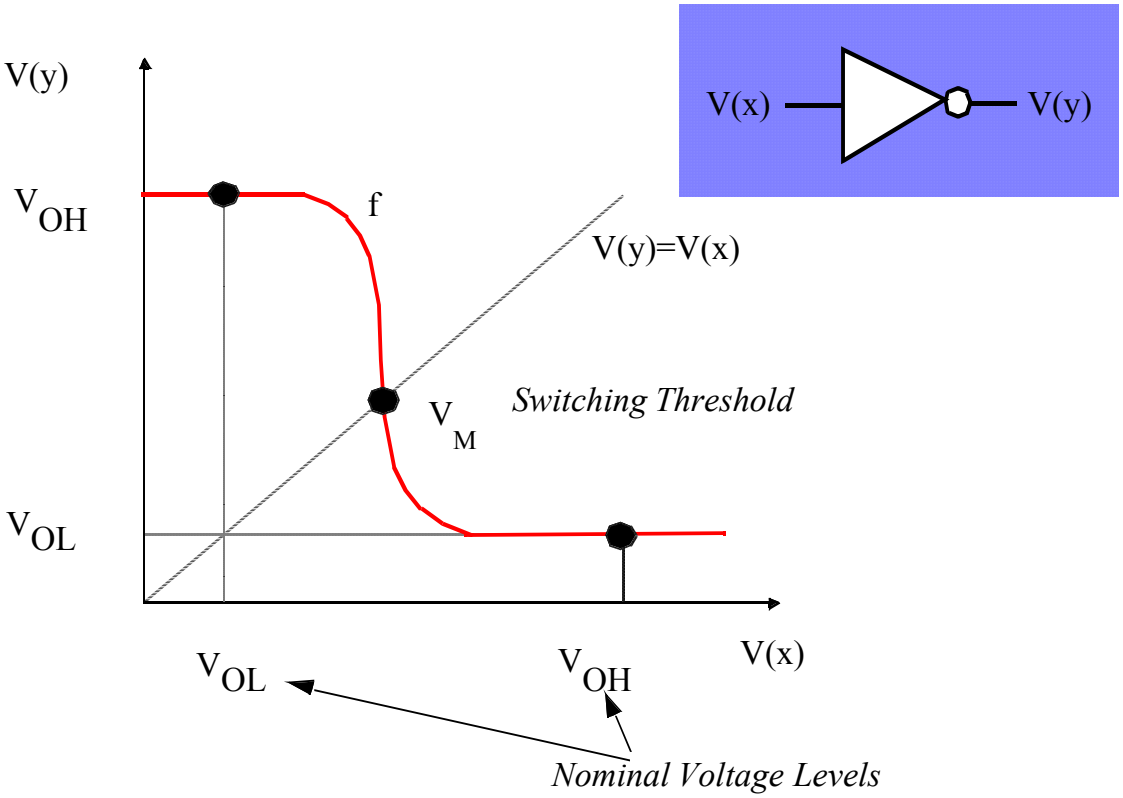
The Ideal Gate



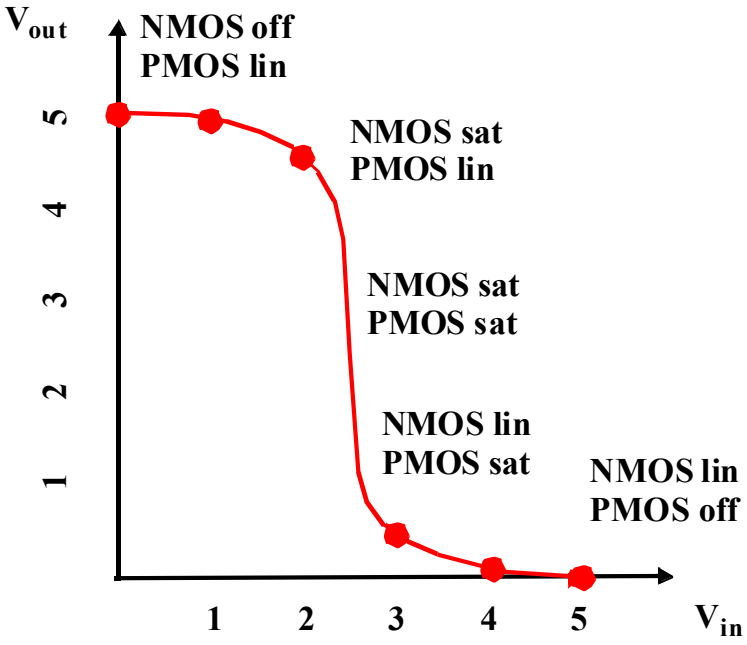
$R_i = \infty$

$R_o = 0$

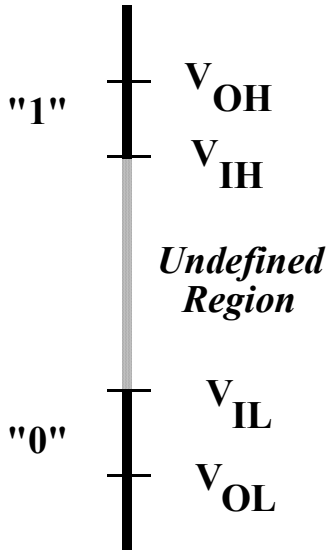
DC Operation: Voltage Transfer Characteristic

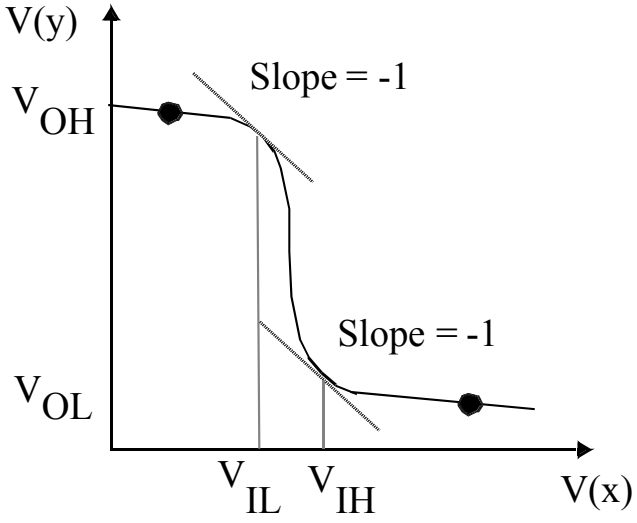


CMOS Inverter VTC

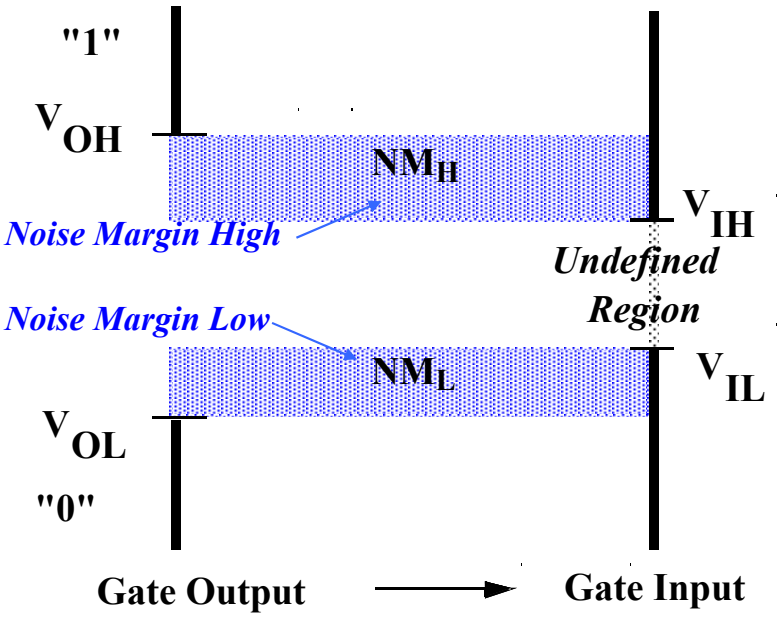


Mapping between analog and digital signals





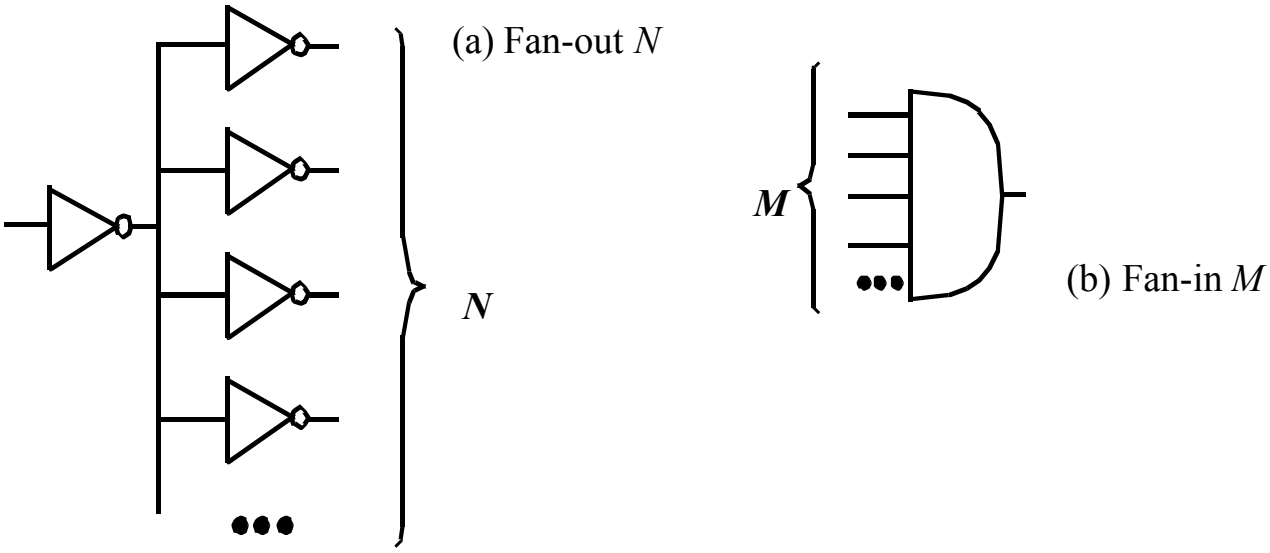
Definition of Noise Margins



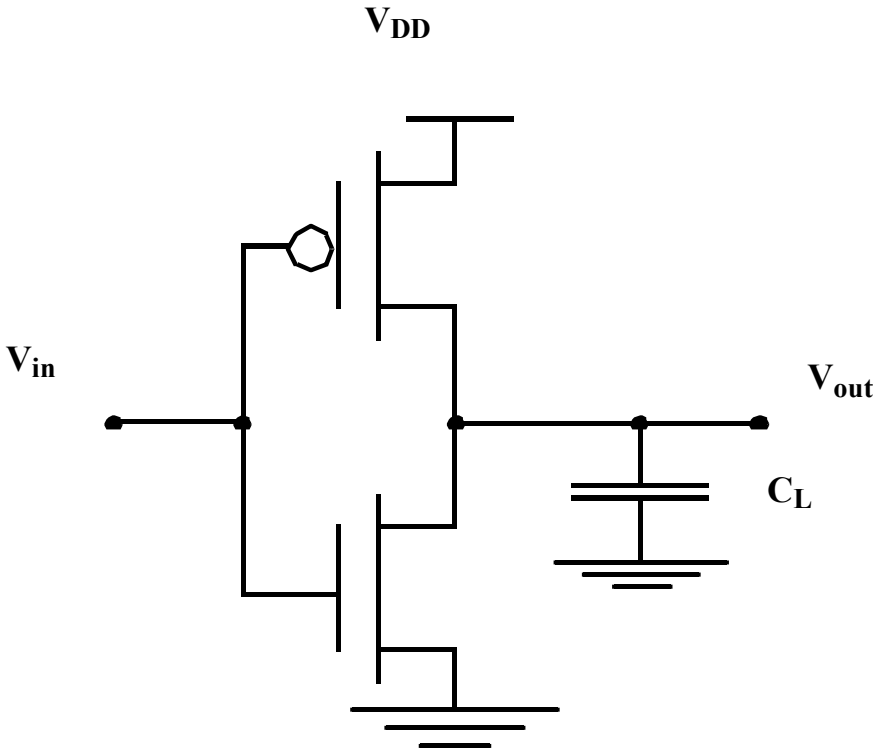
$NM_H = V_{OH} - V_{IH}$ (High input)

$NM_L = V_{OL} - V_{IL}$ (Low input)

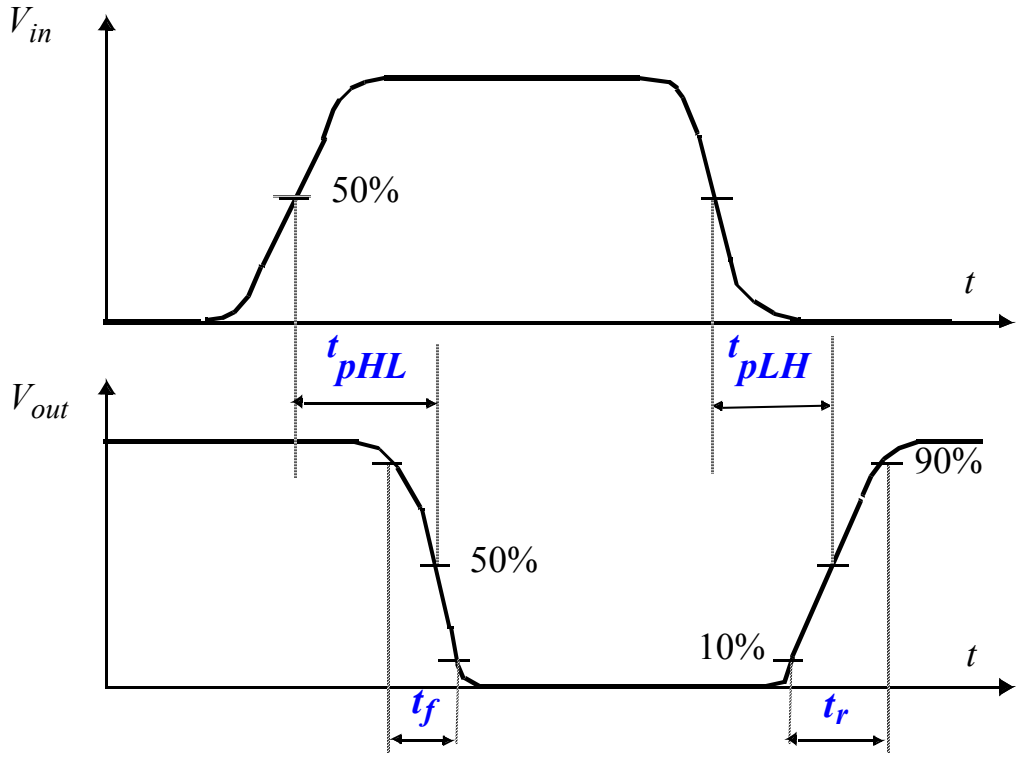
Fan-in and Fan-out



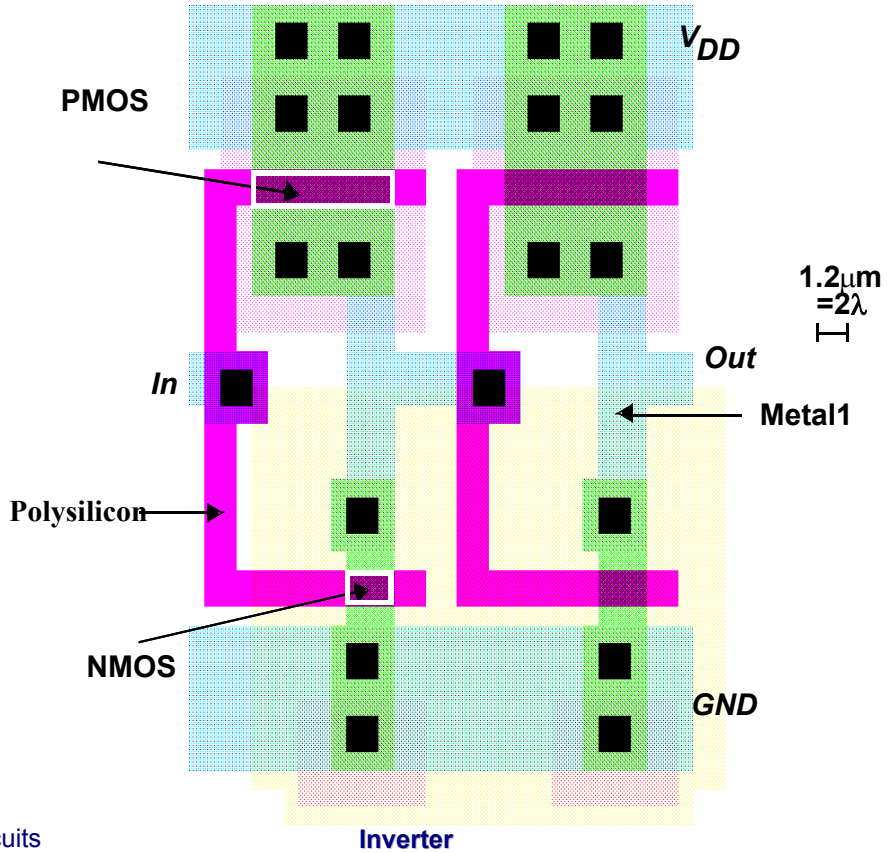
The CMOS Inverter: A First Glance



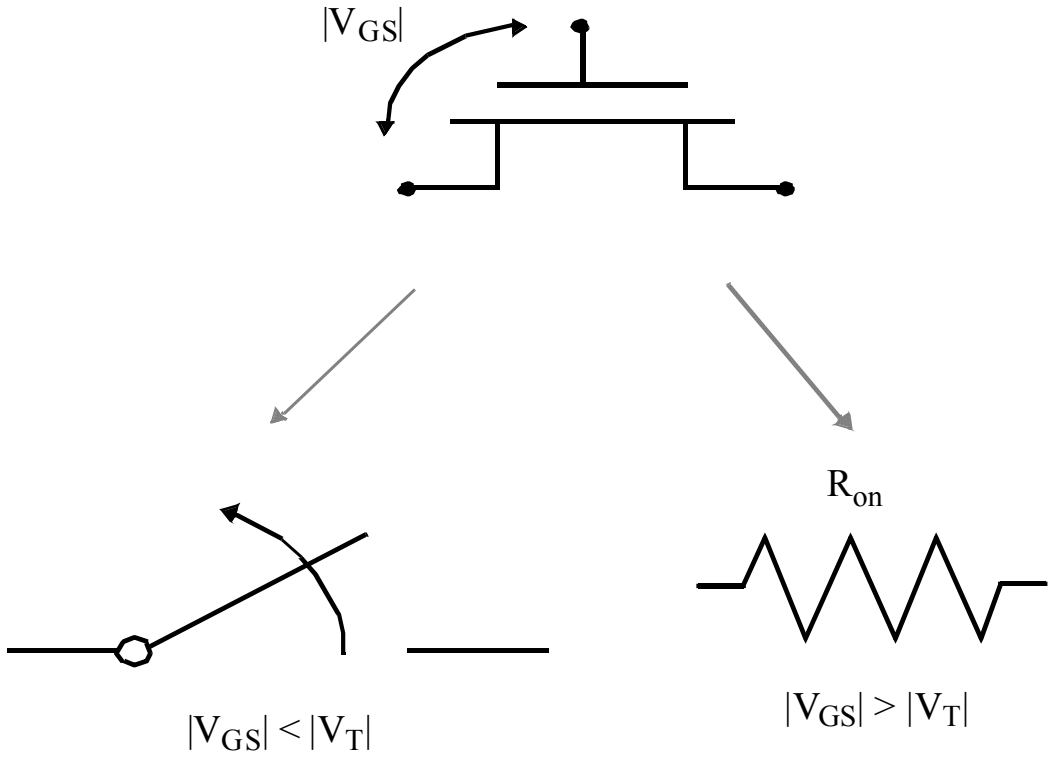
Delay Definitions



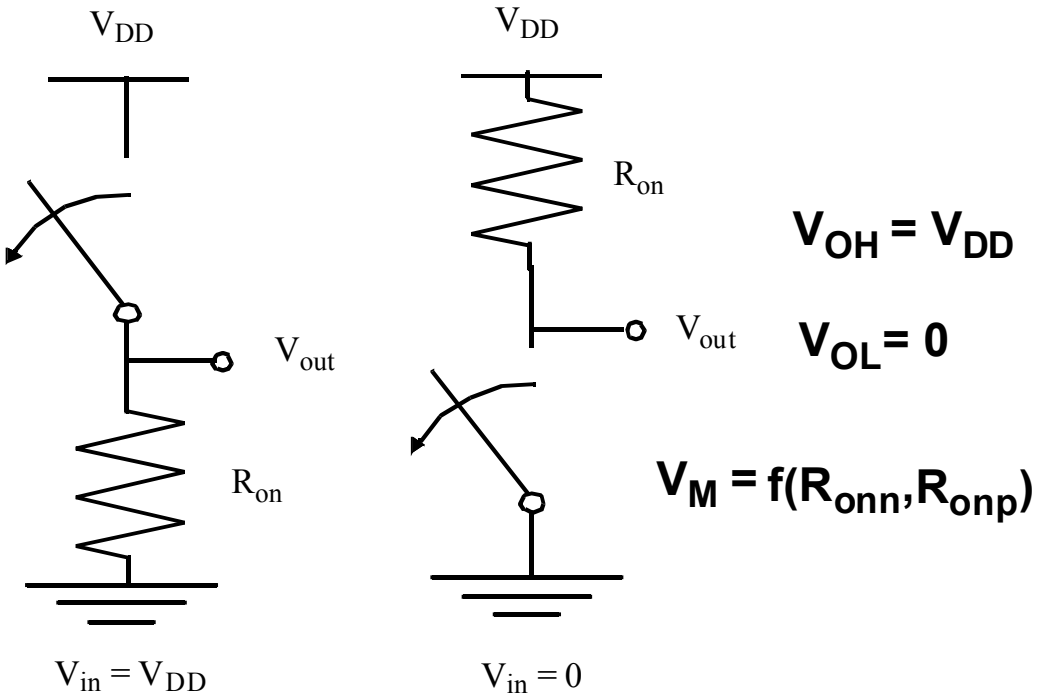
CMOS Inverters



Switch Model of CMOS Transistor



CMOS Inverter: Steady State Response

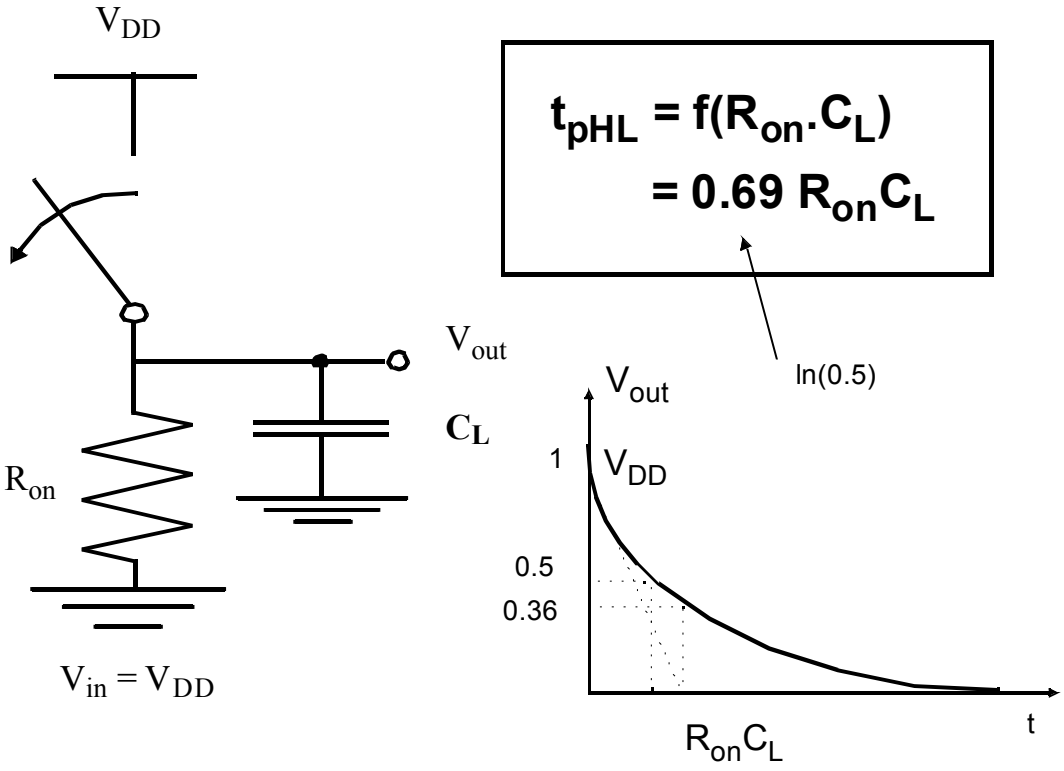


$V_{OH} = V_{DD}$

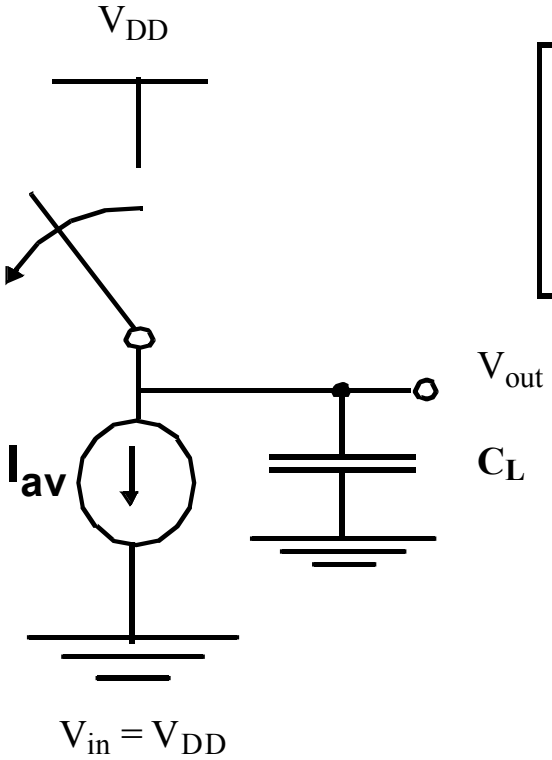
$V_{OL} = 0$

$V_M = f(R_{onn}, R_{onp})$

CMOS Inverter: Transient Response



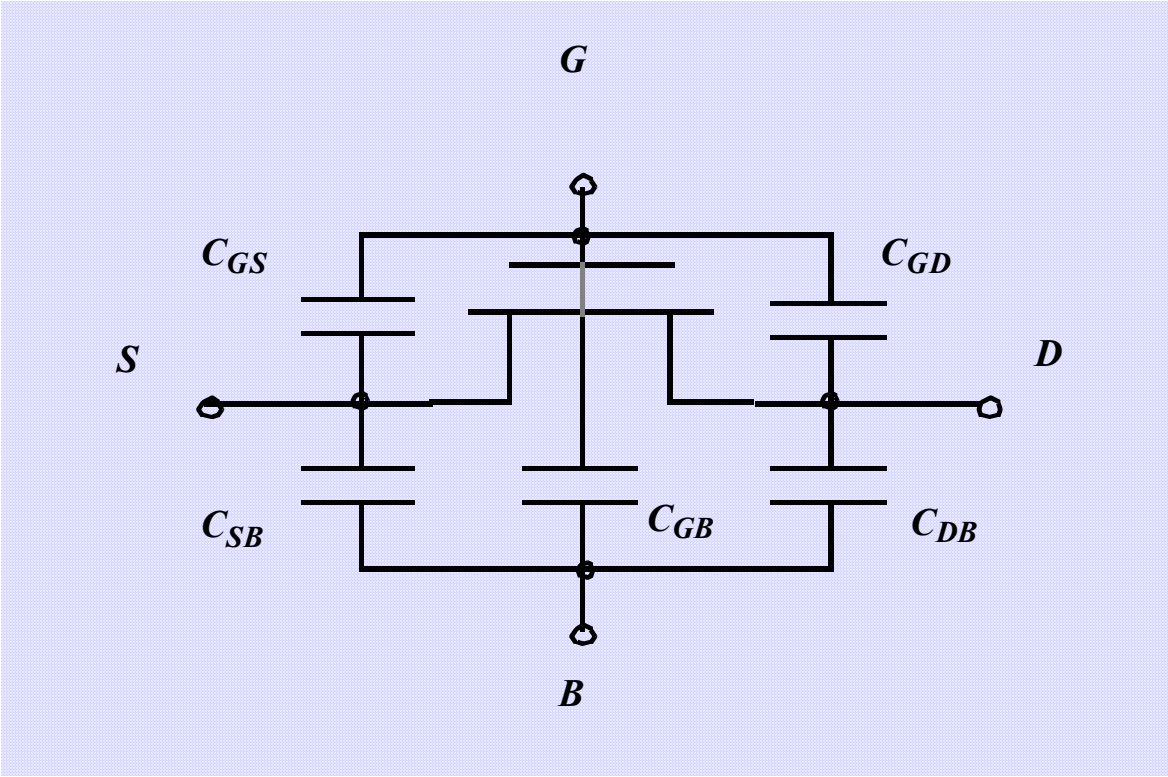
CMOS Inverter Propagation Delay



$$t_{pHL} = \frac{C_L\ V_{swing}/2}{I_{av}}$$

$$\sim \frac{C_L}{k_n\ V_{DD}}$$

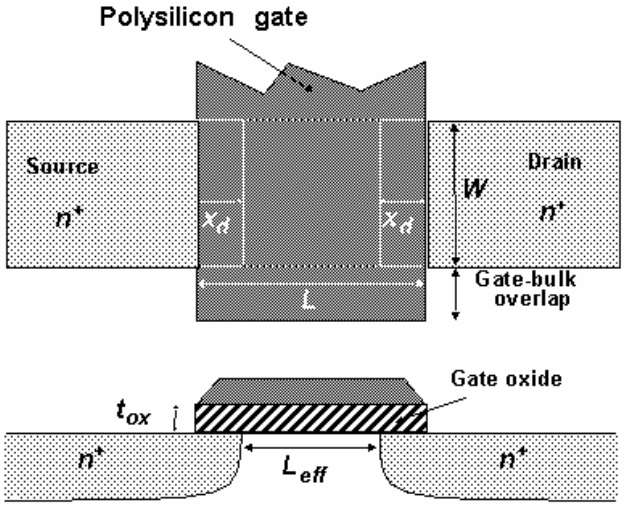
Dynamic Behavior of MOS Transistor



The Gate Capacitance

(a) Top view.

(b) Cross-section



$$C_{gate} = \frac{\varepsilon_{ox}}{t_{ox}} WL$$

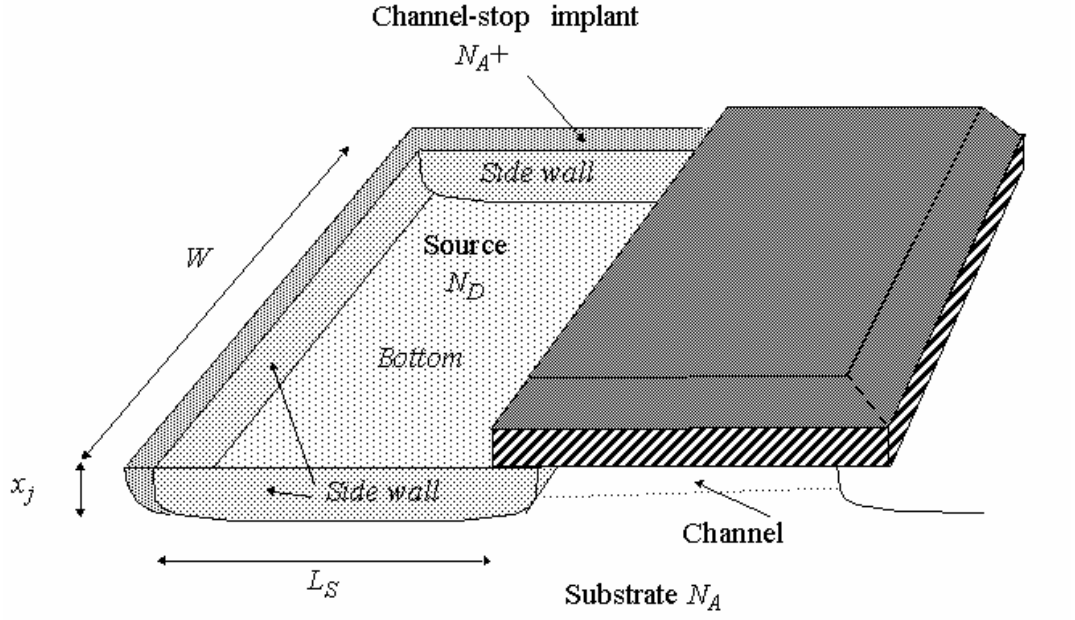
Average Gate Capacitance

Different distributions of gate capacitance for varying operating conditions

Operation Region	C_{gb}	C_{gs}	C_{gd}
Cutoff	$C_{ox}WL_{eff}$	0	0
Triode	0	$C_{ox}WL_{eff}/2$	$C_{ox}WL_{eff}/2$
Saturation	0	$(2/3)C_{ox}WL_{eff}$	0

Most important regions in digital design: saturation and cut-off

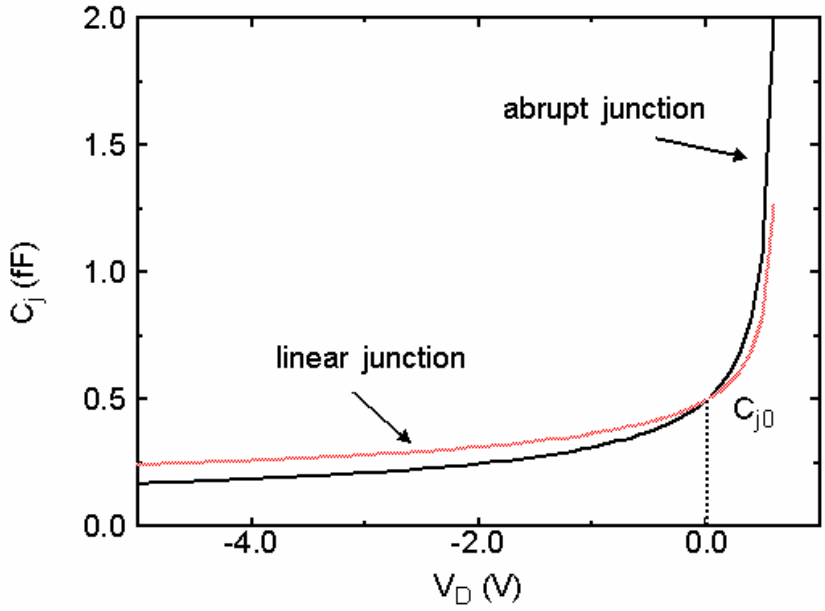
Diffusion Capacitance



$$C_{diff} = C_{bottom} + C_{sw} = C_j \times AREA + C_{jsw} \times PERIMETER$$

$$C_{diff} = C_j L_S W + C_{jsw}(2L_S + 2W)$$

Junction Capacitance



$$C_j = \frac{C_{j0}}{(1 - V_D/\phi_0)^m}$$

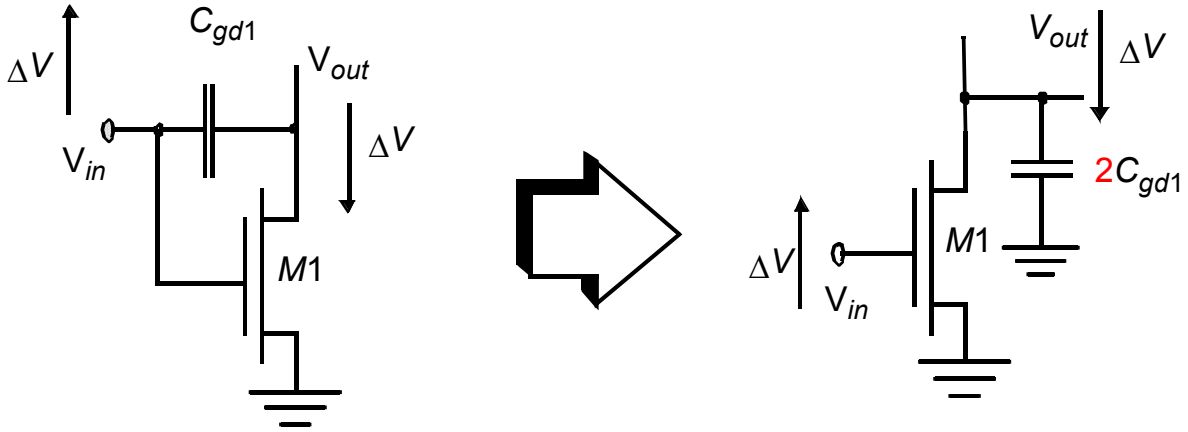
Linearizing the Junction Capacitance

Replace non-linear capacitance by
large-signal equivalent linear capacitance
which displaces equal charge
over voltage swing of interest

$$C_{eq} = \frac{\Delta Q_j}{\Delta V_D} = \frac{Q_j(V_{high}) - Q_j(V_{low})}{V_{high} - V_{low}} = K_{eq} C_{j0}$$

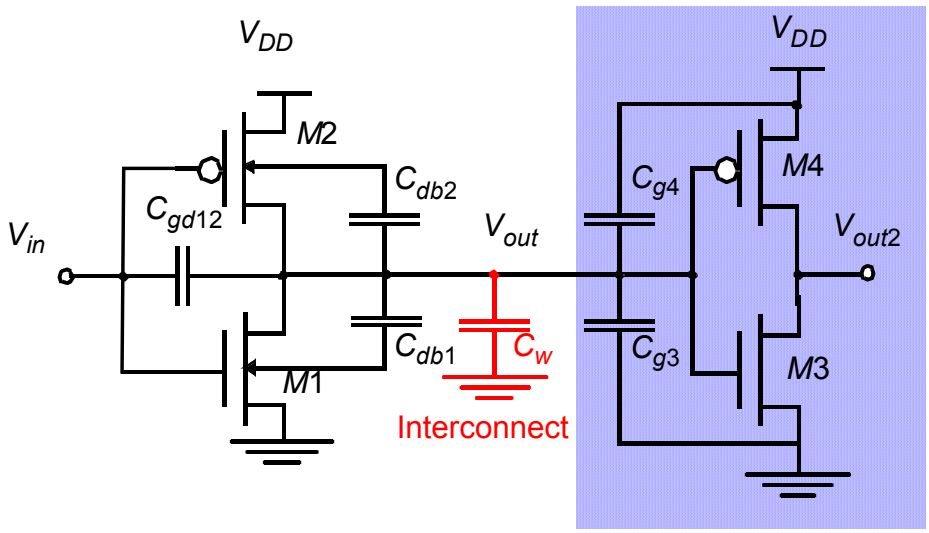
$$K_{eq} = \frac{-\phi_0^m}{(V_{high} - V_{low})(1-m)} [(\phi_0 - V_{high})^{1-m} - (\phi_0 - V_{low})^{1-m}]$$

The Miller Effect

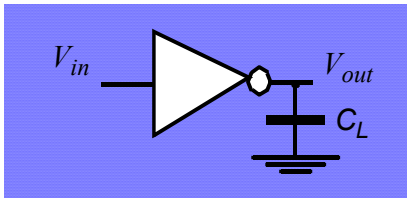


"A capacitor experiencing identical but opposite voltage swings at both its terminals can be replaced by a capacitor to ground, whose value is two times the original value."

Computing the Capacitances



Simplified Model



Computing the Capacitances

Capacitor	Expression
C_{gd1}	2 CGD0 W_n
C_{gd2}	2 CGD0 W_p
C_{db1}	K_{eqn} (AD_n CJ + PD_n CJSW)
C_{db2}	K_{eqp} (AD_p CJ + PD_p CJSW)
C_{g3}	C_{ox} W_n L_n
C_{g4}	C_{ox} W_p L_p
C_w	From Extraction
C_L	Σ

Capacitances: Typical values

Table 3.5 Capacitance parameters of NMOS and PMOS transistors in 0.25 µm CMOS process.

	C_{ox} (fF/µm^2)	C_O (fF/µm)	C_j (fF/µm^2)	m_j	ϕ_b (V)	C_{jsw} (fF/µm)	m_{jsw}	ϕ_{bsw} (V)
NMOS	6	0.31	2	0.5	0.9	0.28	0.44	0.9
PMOS	6	0.27	1.9	0.48	0.9	0.22	0.32	0.9